LSM333D

iNEMO Intertial Module:
9 degrees of freedom sensing solution

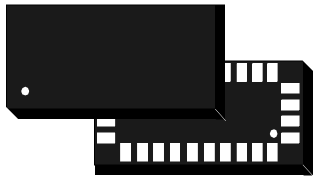
Datasheet — preliminary data

Features

- 3 acceleration channels, 3 angular rate channels, 3 magnetic field channels
- ±2/±4/±8/±16 g dynamically selectable linear acceleration full-scale
- ±2/±4/±8/±12 gauss dynamically selectable magnetic full-scale
- ±250/±500/±2000 dps dynamically selectable angular rate full-scale
- 16-bit data output
- SPI / I²C serial interfaces
- Analog supply voltage 2.4 V to 3.6 V
- Power-down mode / Low-power mode
- Programmable interrupt generators
- Embedded temperature sensor
- Embedded FIFO
- ECOPACK® RoHS and “Green” compliant

Applications

- Indoor navigation
- Smart user interface
- Advanced gesture recognition
- Gaming and virtual reality input device
- Display/map orientation and browsing
- eCompass
- Position and motion detection functions
- Click/double click recognition
- Intelligent power saving for handheld devices



LGA-28 (3.5x6x1 mm)

Description

The LSM333D is an inertial module capable of providing 9 DOF (degrees of freedom) inertial sensing by combining a 3D accelerometer, a 3D gyroscope and a 3D magnetometer in a system-in-package.

The LSM333D has linear acceleration full-scales of ±2*g*/±4*g*/±8*g*/±16*g*, a magnetic field full-scale of ±2/±4/±8/±12 gauss and an angular rate of 250/±500/±2000 dps. All full-scales available are fully selectable by the user.

The LSM333D includes an I²C serial bus interface supporting standard and Fast mode 100 kHz and 400 kHz, and SPI serial standard interface.

The system can be configured to generate interrupt signals, on dedicated pins, motion and magnetic field detection. Thresholds and the timing of interrupt generators are programmable by the end user.

Magnetic, accelerometer and gyroscope sensing can be enabled or set in Power-down mode separately for smart power management.

The LSM333D is available in a plastic land grid array package (LGA) and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

Part number	Temperature range [°C]	Package	Packing
LSM333D	-40 to +85	LGA-28	Tray
LSM333DTR	-40 to +85	LGA-28	Tape and reel

Contents

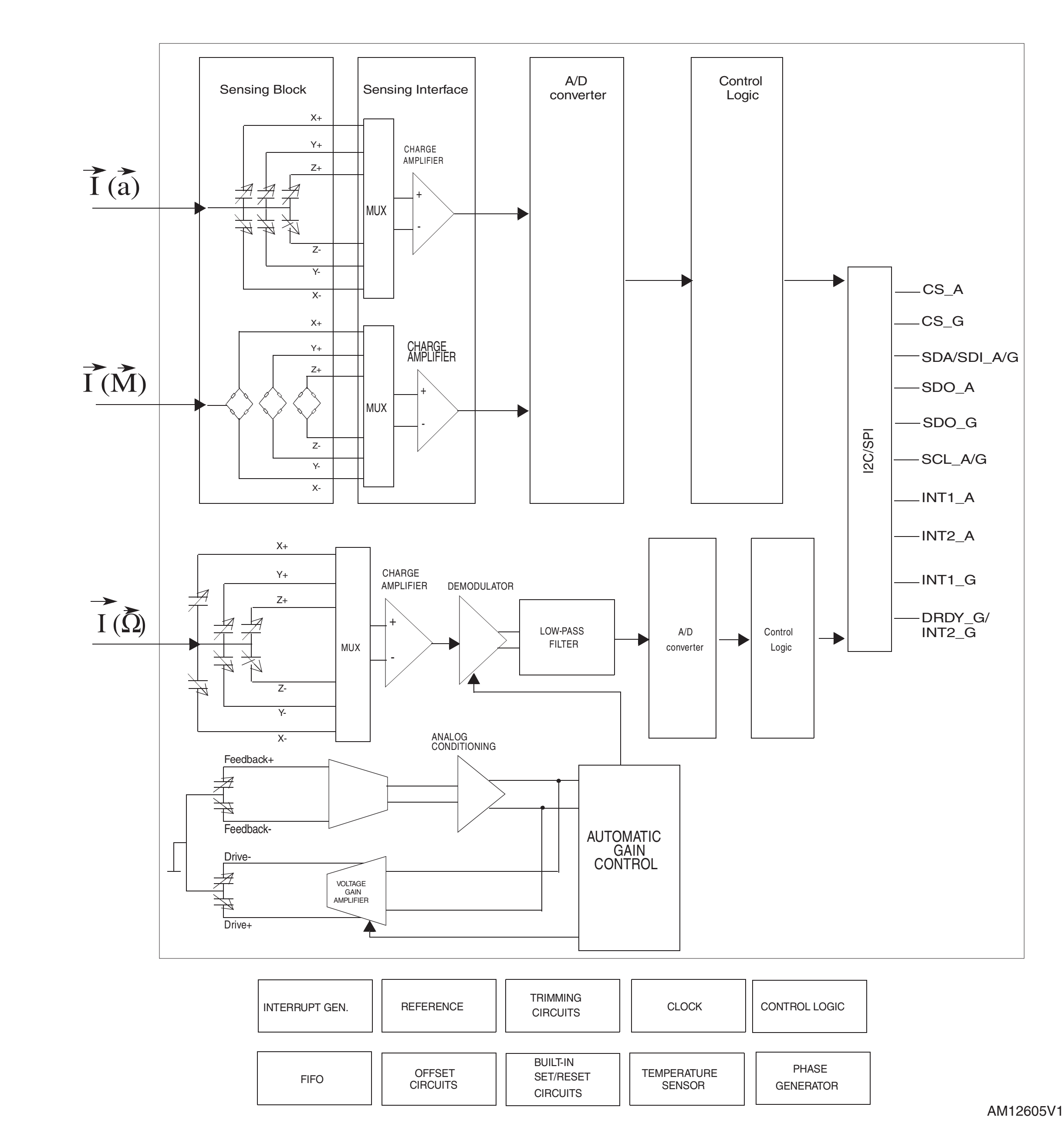
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1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connection

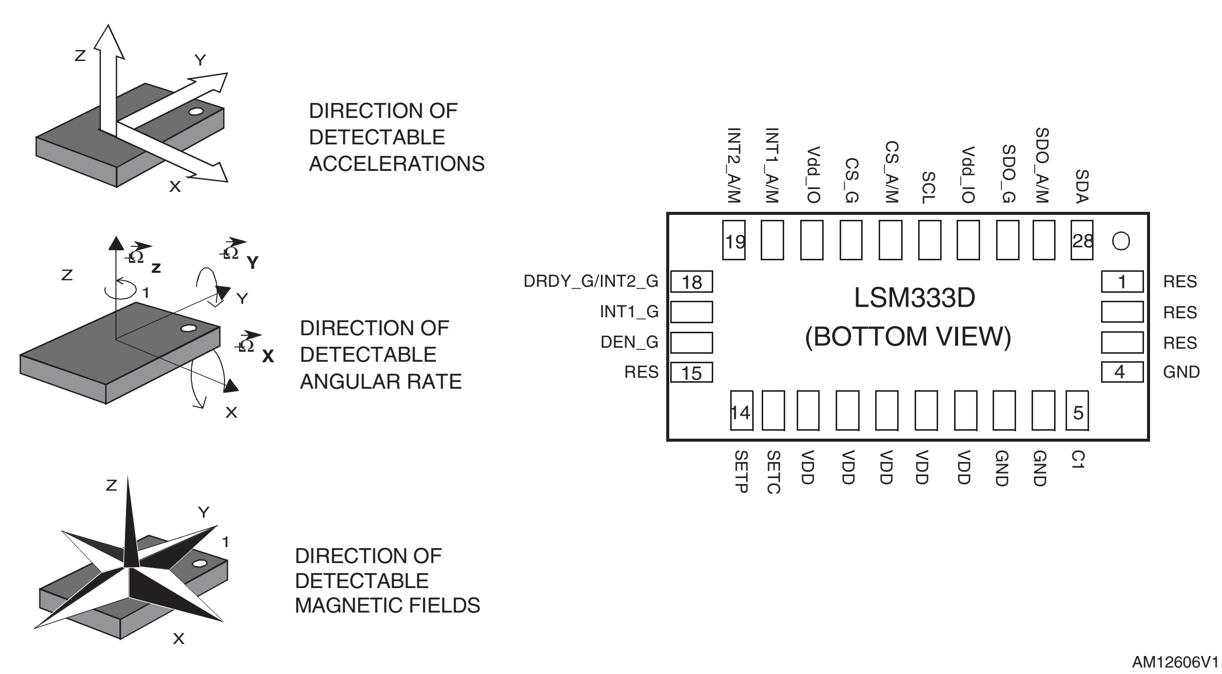


Table 2. Pin description

Pin#	Name	Function
1	Res	Reserved to be connected to GND
2	Res	Reserved to be connected to GND
3	Res	Reserved to be connected to GND
4	GND	0 V supply
5	C1	Capacitor connection (C1)
6	GND	0 V supply
7	GND	0 V supply
8	Vdd	Power supply
9	Vdd	Power supply
10	Vdd	Power supply
11	Vdd	Power supply
12	Vdd	Power supply
13	SETC	S/R capacitor connection (C2)
14	SETP	S/R capacitor connection (C2)
15	Res	Leave unconnected
16	DEN_G	Gyroscope data enable

Table 2. Pin description (continued)

Pin#	Name	Function
17	INT1_G	Gyroscope interrupt signal 1
18	DRDY_G/ INT2_G	Gyroscope data ready/interrupt signal 2
19	INT2_A/M	Accelerometer/Magnetometer interrupt2 signal
20	INT1_A/M	Accelerometer/Magnetometer interrupt1 signal
21	Vdd_IO	Power supply for I/O pins
22	CS_G	Gyroscope: SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
23	CS_A/M	Accelerometer/Magnetometer: SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
24	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
25	Vdd_IO	Power supply for I/O pins
26	SDO_G	Gyroscope: SPI serial data output (SDO) / I^2C least significant bit of the device address (SA0)
27	SDO_A	Accelerometer/Magnetometer:SPI serial data output (SDO) / I^2C least significant bit of the device address (SA0)
28	SDA	I^2C serial data (SDA) / SPI serial data input (SDI) 3-wire interface serial data output (SDO)

2 Module specifications

2.1 Sensor characteristics

@ Vdd = 3.0 V, T = 25 °C unless otherwise noted[a].

Table 3. Sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
LA_FS	Linear acceleration measurement range[2]			±2		g
				±4		
				±8		
				±16		
M_FS	Magnetic measurement range			±2		gauss
				±4		
				±8		
				±12		
G_FS	Angular rate measurement range			±250		dps
				±500		
				±2000		
LA_So	Linear acceleration sensitivity	Linear acceleration FS=±2g		0.06		mg/LSB
		Linear acceleration FS=±4g		0.12		
		Linear acceleration FS=±8g		0.24		
		Linear acceleration FS=±16g		0.73		
M_GN	Magnetic sensitivity	Magnetic FS=±2 gauss		0.08		mgauss/ LSB
		Magnetic FS=±4 gauss		0.16		
		Magnetic FS=±8 gauss		0.32		
		Magnetic FS=±12 gauss		0.48		
G_So	Angular rate sensitivity	Angular rate FS=±250 dps		8.75		mdps/ digit
		Angular rate FS=±500 dps		17.50		
		Angular rate FS=±2000 dps		70		
LA_TCSo	Linear acceleration sensitivity change vs. temperature			±0.01		%/°C
M_TCSo	Magnetic sensitivity change vs. temperature			±0.05		%/°C
G_SoDr	Angular rate sensitivity change vs. temperature	From -40 °C to +85 °C		±2		%

a. The product is factory calibrated at 3.0 V. The operational power supply range is from 2.4 V to 3.6 V.

Table 3. Sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
LA_TyOff	Linear acceleration Typical zero-*g* level offset accuracy(3) (4)			±60		m*g*
G_TyOff	Angular rate Typical zero-rate level	FS = 250 dps		±10		dps
		FS = 500 dps		±15		
		FS = 2000 dps		±25		
LA_TCOff	Linear acceleration zero-*g* level change vs. temperature	Max. delta from 25 °C		±0.5		m*g*/°C
G_TCOff	Zero-rate level change vs. temperature			±0.05		dps/°C
An	Linear acceleration noise density	Linear acceleration FS=2g; ODR = 100Hz		150		ug/ sqrt(Hz)
Mn	Magnetic noise density	Magnetic FS=2gauss; ODR = 100Hz		210		ugauss/ sqrt(Hz)
Rn	Rate noise density	FS = ±250 dps, BW = 50 Hz		0.03		dps/ sqrt(Hz)
M_EF	Maximum exposed field	No permitting effect on zero reading			10000	gauss
M_DF	Magnetic disturbing field	Sensitivity starts to degrade. Automatic S/R pulse restores the sensitivity(5)			20	gauss
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Verified by wafer level test and measurement of initial offset and sensitivity.
3. Typical zero-*g* level offset value after MSL3 preconditioning.
4. Offset can be eliminated by enabling the built-in high-pass filter.
5. Set / reset pulse is automatically applied at each conversion cycle.

2.2 Temperature sensor characteristics

@ Vdd =3.0 V, T=25 °C unless otherwise noted.

Table 4. Electrical characteristics (1)

Symbol	Parameter	Test condition	Min.	Typ.(2)	Max.	Unit
TSDr	Temperature sensor output change vs. temperature	-		-1		°C/digit
TODR	Temperature refresh rate			1		Hz
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 3.0 V.

2. Typical specifications are not guaranteed.

2.3 Electrical characteristics

@ Vdd = 3.0 V, T = 25 °C unless otherwise noted[b].

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
Vdd	Supply voltage		2.4		3.6	V
Vdd_IO	Module power supply for I/O		1.71	1.8	Vdd+0.1	
Idd_A/M	eCompass[2] current consumption in Normal mode [3]			350		µA
Idd_A/M_SL	eCompass current consumption in Power-down mode[4]			1		µA
G_Idd	Gyroscope current consumption in Normal mode			6.1		mA
G_IddLowP	Gyroscope supply current in Sleep mode[5]			2		mA
G_IddPdn	Gyroscope current consumption in Power-down mode			5		µA
VIH	Digital high level input voltage		0.8*Vdd_IO			V
VIL	Digital low level input voltage				0.2*Vdd_IO	V
VOH	High level output voltage		0.9*Vdd_IO			V
VOL	Low level output voltage				0.1*Vdd_IO	V
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. eCompass: accelerometer - magnetic sensor.
3. Magnetic sensor setting ODR =6.25 Hz, accelerometer sensor ODR = 50 Hz.
4. Linear accelerometer and magnetic sensor in Power-down mode.
5. Sleep mode introduces a faster turn-on time compared to Power-down mode.

b. Gyroscope is factory calibrated at 3.0 V.

2.4 Communication interface characteristics

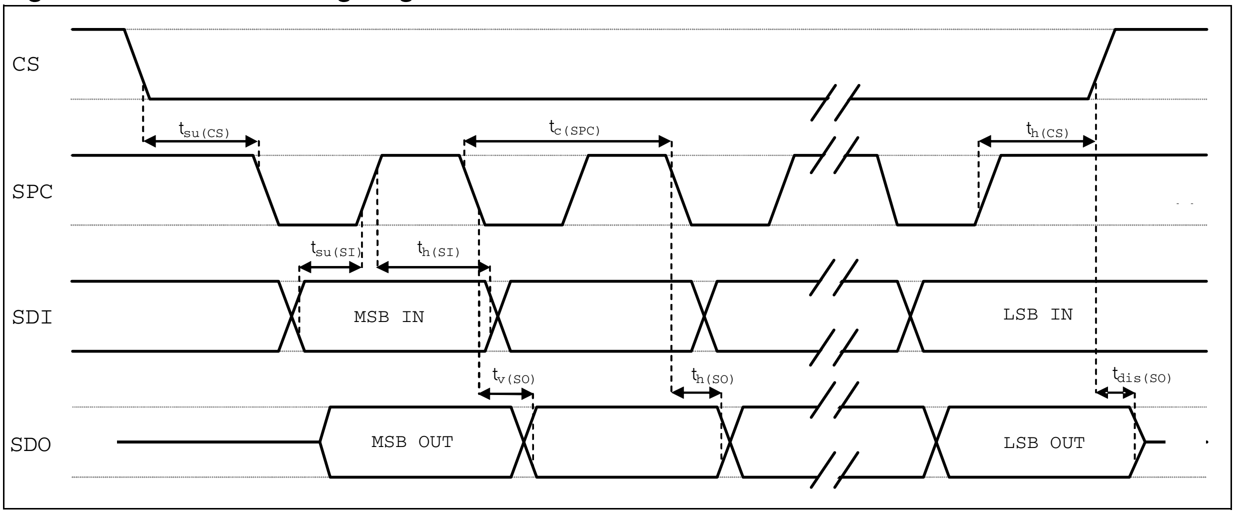
2.4.1 SPI - serial peripheral interface

Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value [(1)]		Unit
		Min.	Max.	
tc(SPC)	SPI clock cycle	100		ns
fc(SPC)	SPI clock frequency		10	MHz
tsu(CS)	CS setup time	5		ns
th(CS)	CS hold time	20		
tsu(SI)	SDI input setup time	5		
th(SI)	SDI input hold time	15		
tv(SO)	SDO valid output time		50	
th(SO)	SDO output hold time	5		
tdis(SO)	SDO output disable time		50	

Figure 3. SPI slave timing diagram [(2)]



1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.
2. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both Input and output ports.

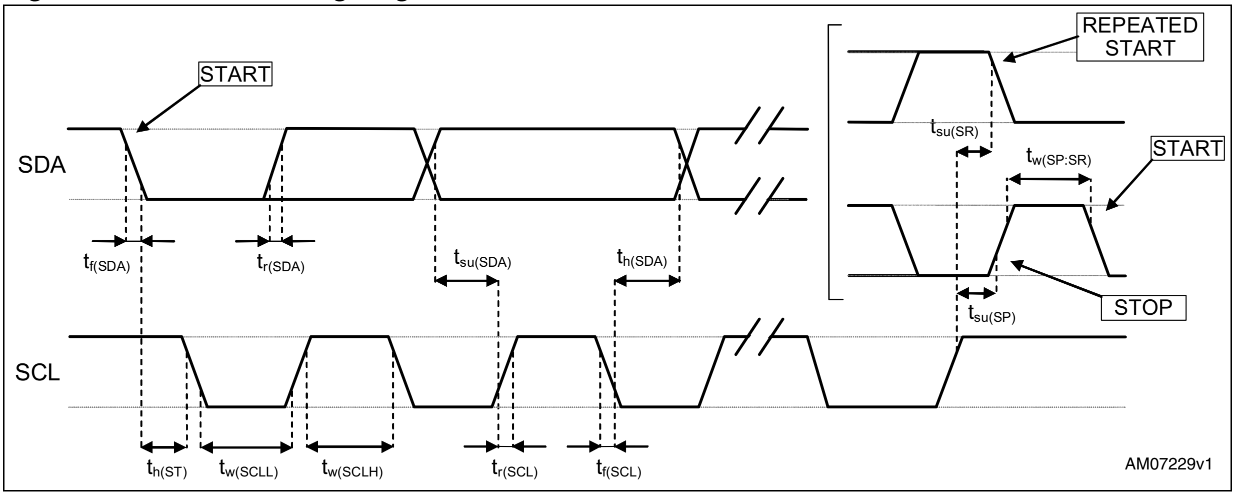
2.4.2 Sensor I²C - inter IC control interface

Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min.	Max.	Min.	Max.	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$ (2)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$ (2)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

Figure 4. I²C slave timing diagram (3)



1. Data based on standard I²C protocol requirement, not tested in production.
2. Cb = total capacitance of one bus line, in pF.
3. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (SCL, SDA, SDO_A/M, SDO_G, CS_G, CS_A/M, DEN_G)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 2.5 V)	3,000 for 0.5 ms	*g*
		10,000 for 0.1 ms	*g*
A_{UNP}	Acceleration (any axis, unpowered)	3,000 for 0.5 ms	*g*
		10,000 for 0.1 ms	*g*
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V.

This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part

This is an ESD sensitive device, improper handling can cause permanent damage to the part

3 Terminology

3.1 Set/Reset pulse

The set/reset pulse is an automatic operation performed before each magnetic acquisition cycle to de-gauss the sensor and to ensure alignment of the magnetic dipoles and therefore the linearity of the sensor itself.

3.2 Sensitivity

3.2.1 Linear acceleration sensor sensitivity

Linear acceleration sensitivity describes the gain of the sensor and can be determined e.g. by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations, this can be done easily by pointing the axis of interest towards the center of the earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and also time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

3.2.2 Angular rate sensor sensitivity

An angular rate gyroscope is a device that produces a positive-going digital output for counter-clockwise rotation around the sensitive axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

3.2.3 Magnetic sensor sensitivity

Sensitivity describes the gain of the sensor and can be determined e.g. by applying a magnetic field of 1 *gauss* to it.

3.3 Zero-*g* level

Zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady-state on a horizontal surface measures 0 *g* in the X-axis and 0 *g* in the Y-axis, whereas the Z-axis measures 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2’s complement number). A deviation from the ideal value in this case is called zero-*g* offset. Offset is to some extent a result of stress to the MEMS sensor and therefore can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see “Zero-*g* level change vs. temperature”. The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a population of sensors.

3.4 Zero-rate level

Zero-rate level describes the actual output signal if there is no angular rate present. Zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and time.

3.5 Zero-*gauss* level

Zero-*g*auss level offset describes the deviation of an actual output signal from the ideal output if no magnetic field is present. Thanks to the set/reset pulse and to the magnetic sensor readout chain, the offset is dynamically cancelled. The zero-*g*auss level does not show any dependencies from temperature and power supply.

4 Functionality

The LSM333D is a system-in-package featuring a 3D digital accelerometer, a 3D digital Magnetometer, and a 3D digital gyroscope.

The device includes specific sensing elements and two IC interfaces capable of measuring both the acceleration/Magnetometer and angular rate applied to the module and to provide a signal to external applications through an SPI/I^{2}C serial interface.

The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using a CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LSM333D may also be configured to generate an inertial *wake-up* and *free-fall* interrupt signal according to a programmed acceleration event along the enabled axes.

4.1 Accelerometer / Gyroscope self-test

Self-test allows the linear acceleration sensor functionality to be tested without moving it. The self-test function is off when the self-test bit (ST) is programmed to ‘0’. When the self-test bit is programmed to ‘1’ an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs exhibit a change in their DC levels which are related to the selected full-scale through the device sensitivity. When self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified inside *Section 2.1: Sensor characteristics*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

4.2 Linear acceleration digital main blocks

4.2.1 FIFO

The LSM333D embeds 32 slots of data FIFO for each of the three output channels: X, Y and Z. This allows a consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work accordingly in four different modes: Bypass mode, FIFO mode, Stream mode and Stream-to-FIFO mode. Each mode is selected by the FIFO_MODE bits in *FIFO_SRC_REG_A (2Fh)*. Programmable watermark level, FIFO_Empty or FIFO_Full events can be enabled to generate dedicated interrupts on the INT1_A/INT2_A pin (configured through *FIFO_SRC_REG_A (2Fh)*).

4.2.2 Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. For each channel only the first address is used. The remaining FIFO slots are empty.

4.2.3 FIFO mode

In FIFO mode, data from the X, Y and Z channels are stored in the FIFO. A watermark interrupt can be enabled (FIFO_WTMK_EN bit in *FIFO_CNTRL_REG_A (2Eh)*) in order to be raised when the FIFO is filled to the level specified in the FIFO_WTMK_LEVEL bits of *FIFO_CNTRL_REG_A (2Eh)*. The FIFO continues filling until it is full (32 slots of data for X, Y and Z). When full, the FIFO stops collecting data from the input channels.

4.2.4 Stream mode

In Stream mode, data from the X, Y and Z measurement are stored in the FIFO. A watermark interrupt can be enabled and set as in FIFO mode. The FIFO continues filling until it is full (32 slots of data for X, Y and Z). When full, the FIFO discards the older data as the new data arrives.

4.2.5 Stream-to-FIFO mode

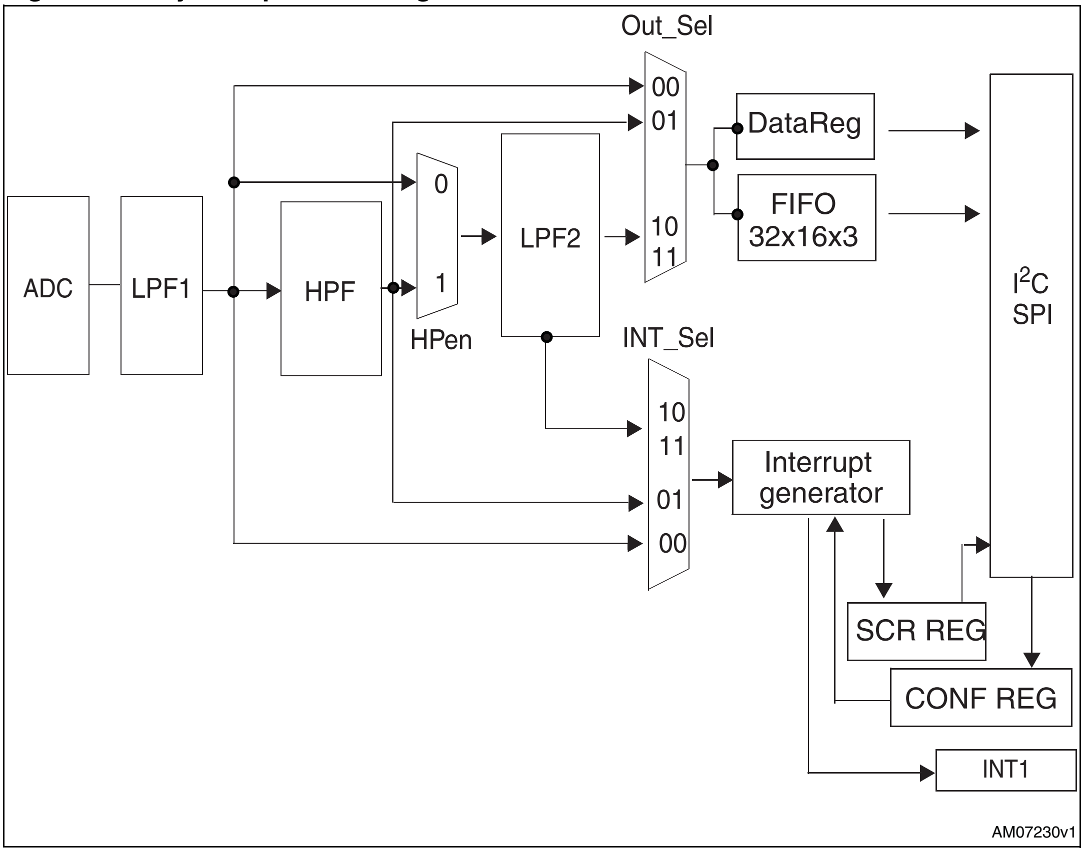
In Stream-to-FIFO mode, data from the X, Y and Z measurement is stored in the FIFO. A watermark interrupt can be enabled (FIFO_WTMK_EN bit in *FIFO_CNTRL_REG_A (2Eh)*) in order to be raised when the FIFO is filled to the level specified in the FIFO_WTMK_LEVEL bits of *FIFO_CNTRL_REG_A (2Eh)*. The FIFO continues filling until it is full (32 slots of 8-bit data for X, Y and Z). When full, the FIFO discards the older data as the data new arrives. Once a trigger event occurs, the FIFO starts operating in FIFO mode.

4.2.6 Retrieve data from FIFO

FIFO data is read through *OUT_X_L_A (28h), OUT_X_H_A (29h)*, *OUT_Y_L_A (2Ah), OUT_X_H_A (2Bh)* and *OUT_X_L_A (2Ch), OUT_X_H_A (2Dh)*. When the FIFO is in Stream, Trigger or FIFO mode, a read operation to the *OUT_X_L_A (28h), OUT_X_H_A (29h)*, *OUT_Y_L_A (2Ah), OUT_X_H_A (2Bh)* or *OUT_X_L_A (2Ch), OUT_X_H_A (2Dh)* registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest X, Y and Z data are placed in the *OUT_X_L_A (28h), OUT_X_H_A (29h)*, *OUT_Y_L_A (2Ah), OUT_X_H_A (2Bh)* and *OUT_X_L_A (2Ch), OUT_X_H_A (2Dh)* registers and both single read and read_burst operations can be used.

4.3 Gyroscope digital main blocks

Figure 5. Gyroscope block diagram



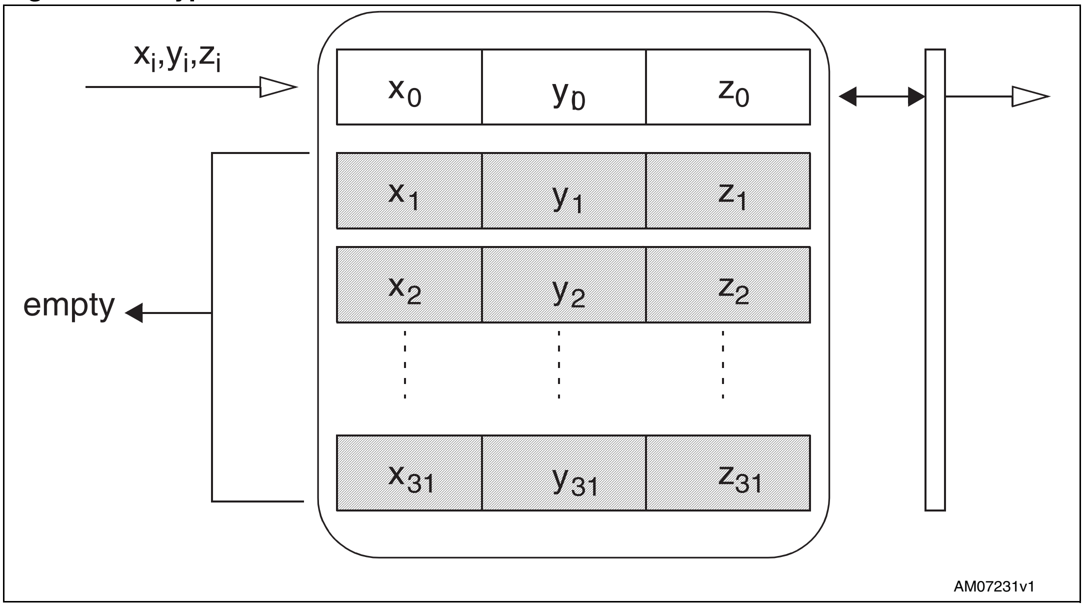
4.3.1 FIFO

The LSM333D embeds 32 slots of 16-bit data FIFO for each of the three output channels: yaw, pitch and roll. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but can wake up only when needed and burst the significant data out from the FIFO. This buffer can work accordingly in five different modes: Bypass mode, FIFO mode, Stream mode, Bypass-to-Stream mode and Stream-to-FIFO mode. Each mode is selected by the FIFO_MODE bits in *FIFO_CTRL_REG_G (2Eh)*. Programmable watermark level, FIFO_Empty or FIFO_Full events can be enabled to generate dedicated interrupts on the DRDY_G/INT2_G pin (configured through *CNTRL3_G (22h)* and event detection information is available in *FIFO_SRC_REG_G (2Fh)*. Watermark level can be configured to WTM4:0 in *FIFO_CTRL_REG_G (2Eh)*.

4.3.2 Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. As described in *Figure 6* below, for each channel only the first address is used. The remaining FIFO slots are empty. When new data is available the old data is overwritten.

Figure 6. Bypass mode

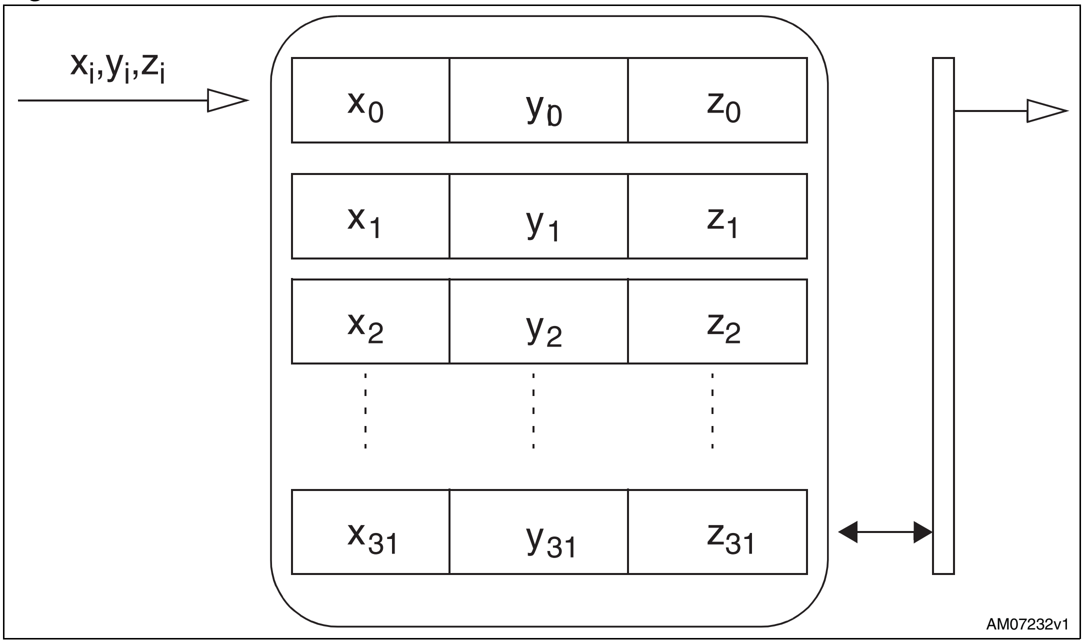


4.3.3 FIFO mode

In FIFO mode, data from the yaw, pitch and roll channels is stored in the FIFO. A watermark interrupt can be enabled (I2_WMK bit in *CNTRL3_G (22h)*) in order to be raised when the FIFO is filled to the level specified in the WTM 4:0 bits of *FIFO_CTRL_REG_G (2Eh)*. The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO stops collecting data from the input channels. To restart data collection, *FIFO_CTRL_REG_G (2Eh)* must be written back to Bypass mode.

FIFO mode is represented in *Figure 7*.

Figure 7. FIFO mode

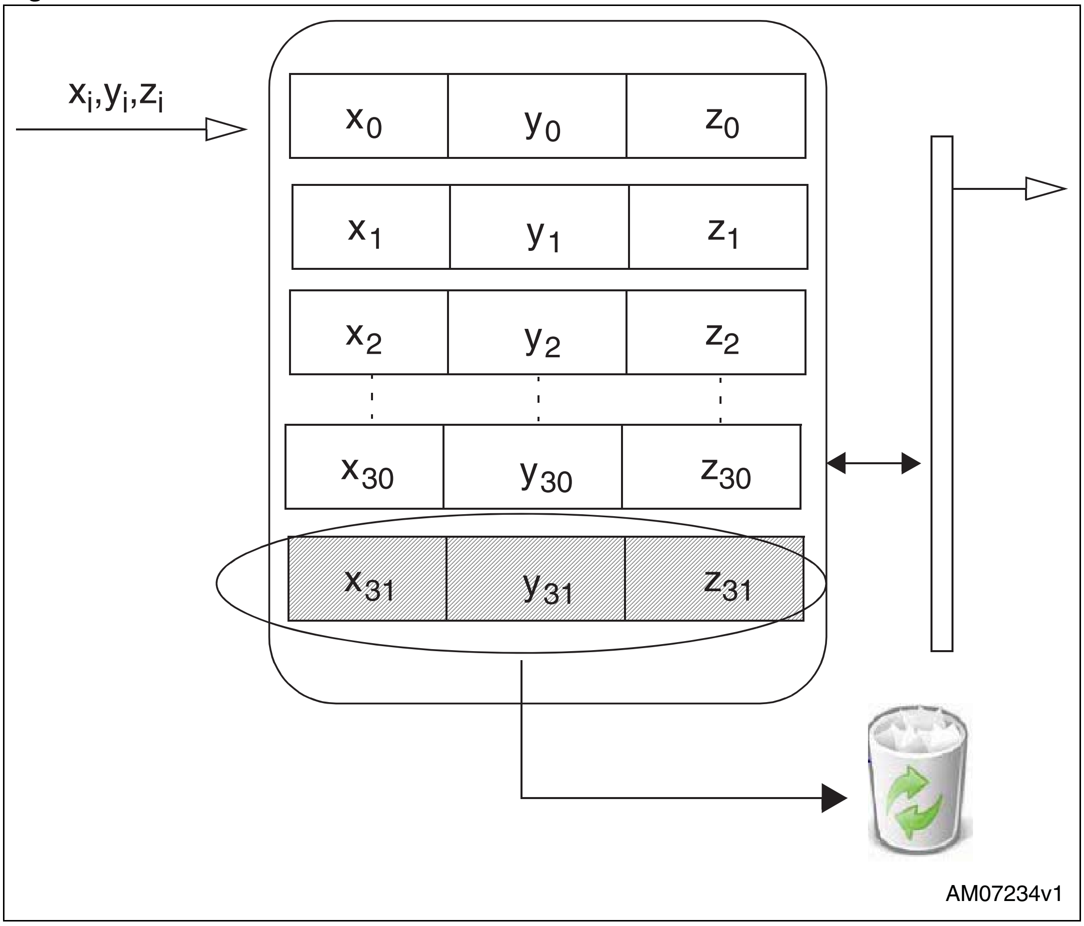


4.3.4 Stream mode

In Stream mode, data from the yaw, pitch and roll measurement is stored in the FIFO. A watermark interrupt can be enabled and set as in FIFO mode. The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO discards the older data as the new data arrives. Programmable watermark level events can be enabled to generate dedicated interrupts on the DRDY_G/INT2_G pin (configured through *CNTRL3_G (22h)*.

Stream mode is represented in *Figure 8*.

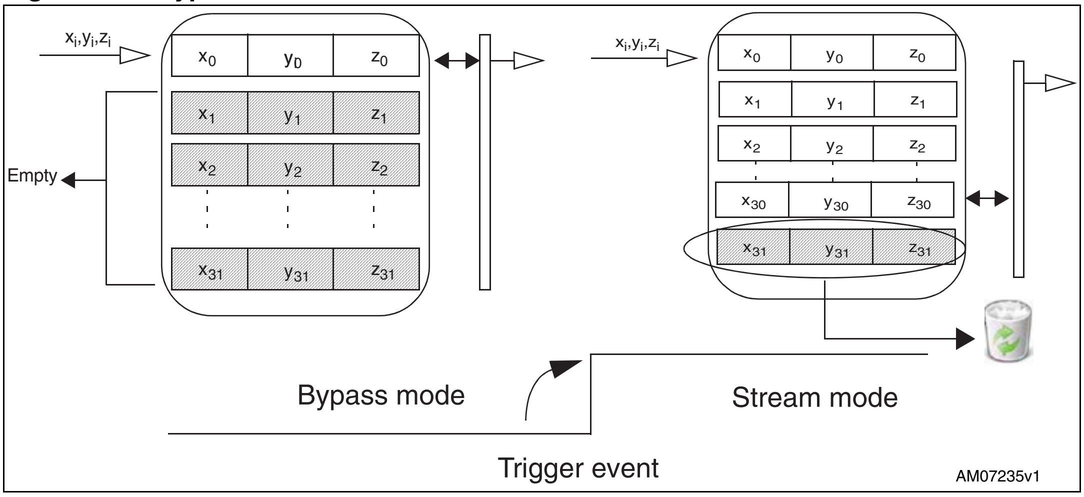
Figure 8. Stream mode



4.3.5 Bypass-to-stream mode

In Bypass-to-stream mode, the FIFO starts operating in Bypass mode and once a trigger event occurs (related to *INT1_CFG_G (30h)* events) the FIFO starts operating in Stream mode. Refer to *Figure 9* below.

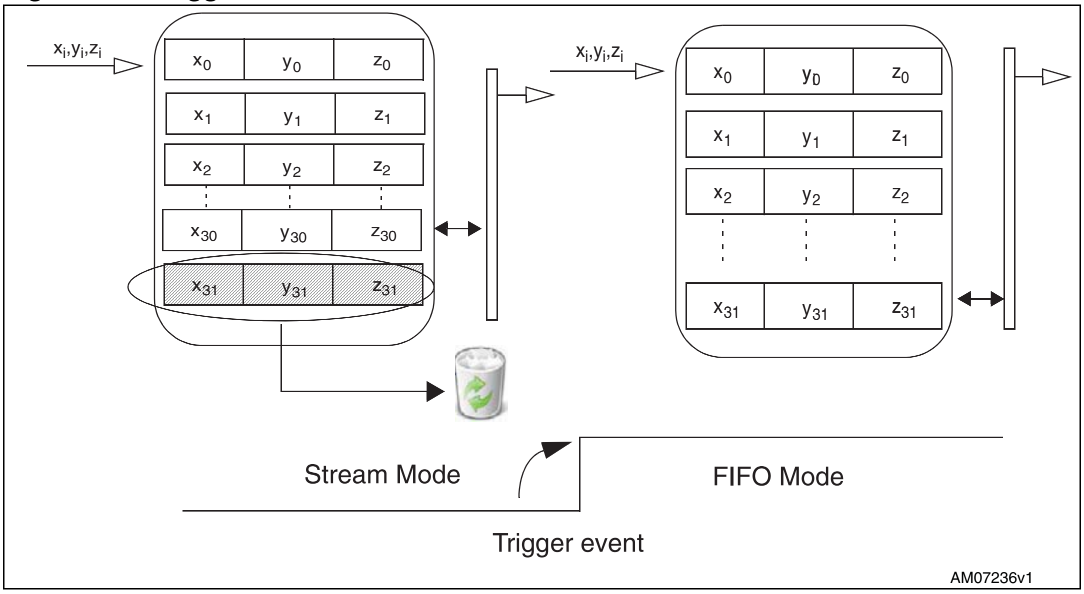
Figure 9. Bypass-to-stream mode



4.3.6 Stream-to-FIFO mode

In Stream-to-FIFO mode, data from the yaw, pitch and roll measurement is stored in the FIFO. A watermark interrupt can be enabled on pin DRDY/INT2 by setting the I2_WTM bit in *CNTRL3_G (22h)* to be raised when the FIFO is filled to the level specified in the WTM4:0 bits of *FIFO_CTRL_REG_G (2Eh)*. The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO discards the older data as the new data arrives. Once a trigger event occurs (related to *INT1_CFG_G (30h)* events), the FIFO starts operating in FIFO mode. Refer to *Figure 10*.

Figure 10. Trigger stream mode



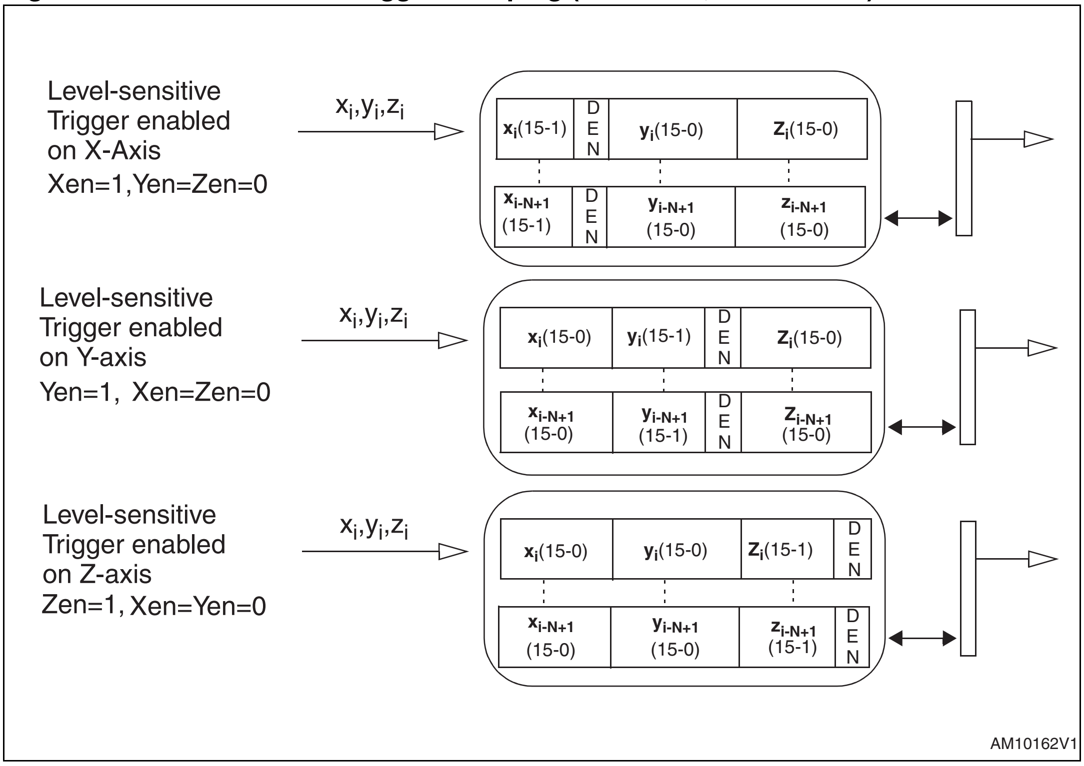
4.3.7 Retrieve data from FIFO

FIFO data is read through *OUT_X_L_G (28h), OUT_X_H_G (29h)*, *OUT_Y_L_G (2Ah), OUT_Y_H_G (2Bh)* and *OUT_Z_L_G (2Ch), OUT_Z_H_G (2Dh)*. When the FIFO is in Stream, Trigger or FIFO mode, a read operation to the *OUT_X_L_G (28h), OUT_X_H_G (29h)*, *OUT_Y_L_G (2Ah), OUT_Y_H_G (2Bh)* or *OUT_Z_L_G (2Ch), OUT_Z_H_G (2Dh)* registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest pitch, roll and yaw data are placed in the *OUT_X_L_G (28h), OUT_X_H_G (29h)*, *OUT_Y_L_G (2Ah), OUT_Y_H_G (2Bh)* and *OUT_Z_L_G (2Ch), OUT_Z_H_G (2Dh)* registers and both single read and read_burst (X,Y & Z with auto-incremental address) operations can be used. When data included in *OUT_Z_H_G* is read, the system again starts to read information from addr *OUT_X_L_G*.

4.4 Level-sensitive / edge-sensitive data enable

The LSM333D allows external trigger level recognition through the enabling of the EXTRen and LVLen bits in *CNTRL2_G (21h)*. Two different modes can be used: Level-sensitive or Edge-sensitive trigger.

Figure 11. Level-sensitive trigger stamping (LVLen = 1; EXTRen = 0)



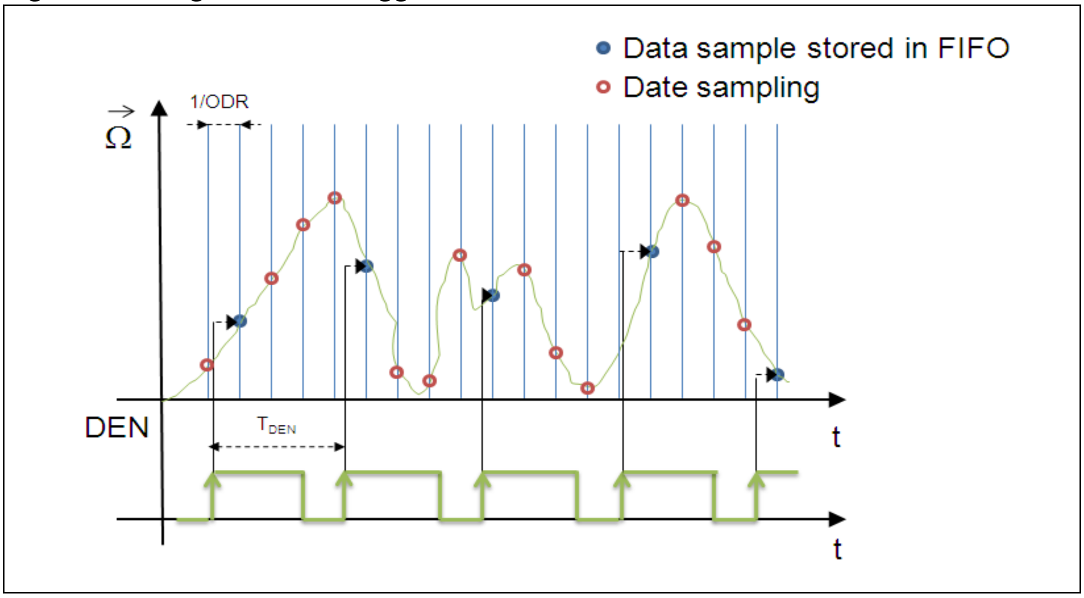
4.4.1 Level-sensitive trigger stamping

Once enabled, the DEN level replaces the LSb of the X, Y or Z axes, configurable through the Xen, Yen, and Zen bits in *CNTRL1_G (20h)*. Data is stored in the FIFO with the internally-selected ODR.

4.4.2 Edge-sensitive trigger

Once enabled by setting EXTRen = 1, FIFO is filled with the pitch, roll and yaw data on the rising edge of the DEN input signal. When the selected ODR is 800 Hz, the maximum DEN sample frequency is $f_{DEN} = 1/T_{DEN} = 400$ Hz.

Figure 12. Edge-sensitive trigger



4.5 Temperature sensor

The LSM333D features an internal temperature sensor. Temperature data can be enabled by setting the TEMP_EN bit on the *CNTRL7_A (26h)* register to 1.

Both OUT_TEMP_H and OUT_TEMP_L registers must be read.

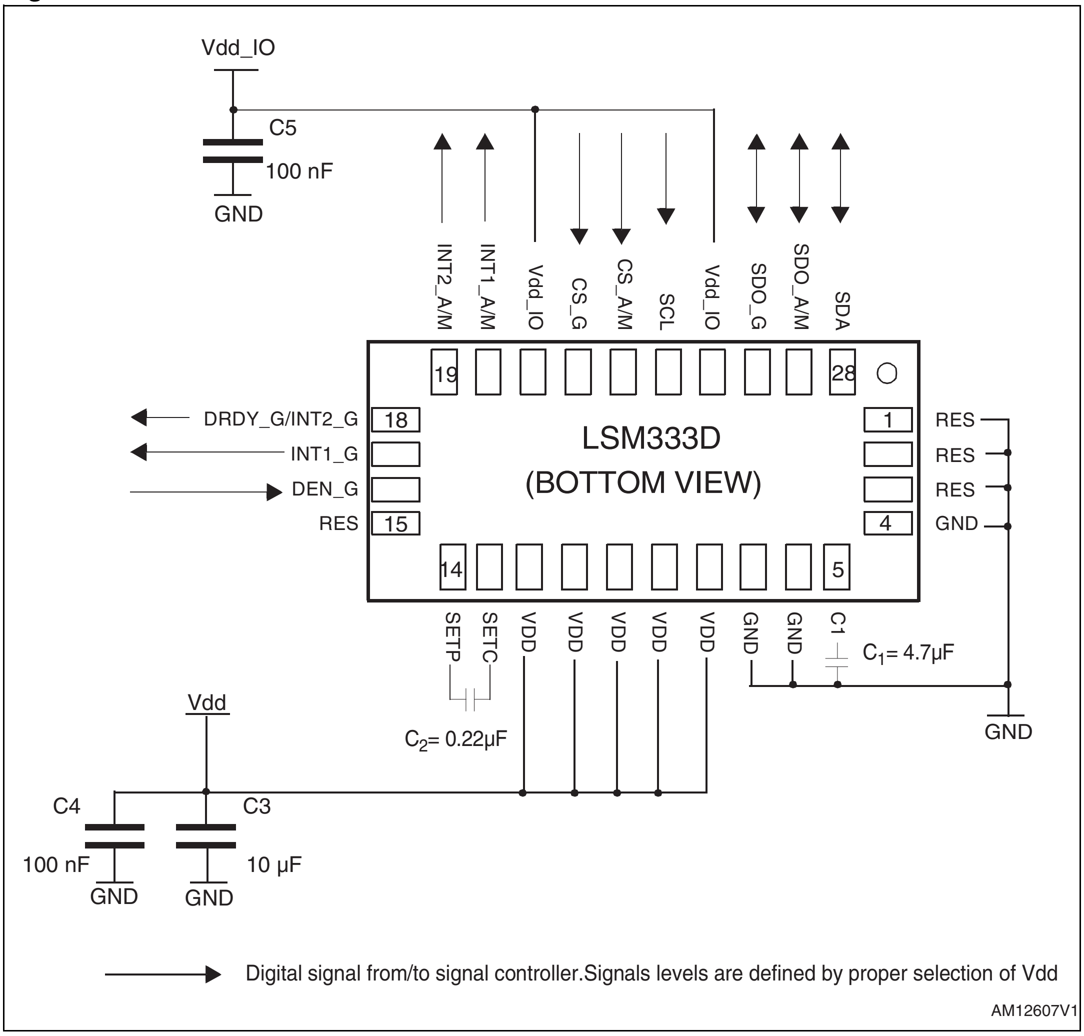
Temperature data is stored inside *STATUS_REG_M (07h)* as 2's complement data in 12-bit format, right justified. The output data rate of the temperature sensor is set by M_ODR in *CNTRL5_A (24h)* and is equal the magnetic sensor output data rate.

4.6 Factory calibration

The IC interface is factory calibrated. The trimming values are stored inside the device by a non-volatile memory. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during normal operation. This allows the user to use the device without further calibration.

5 Application hints

Figure 13. LSM333D electrical connection



5.1 External capacitors

The C1 and C2 external capacitors should be of a low SR value ceramic type construction (typ. suggested value 200 mOhm). Reservoir capacitor C1 is nominally 4.7 µF in capacitance, with the set/reset capacitor C2 nominally 0.22 µF in capacitance.

The device core is supplied through the Vdd line. Power supply decoupling capacitors (C5=C4=100 *nF* ceramic, C3=10 *µF* Al) should be placed as near as possible to the supply pin of the device (common design practice). All the voltage and ground supplies must be present at the same time to achieve proper behavior of the IC (refer to *Figure 13*).

The functionality of the device and the measured acceleration/magnetic field data is selectable and accessible through the I^2C/SPI interfaces.

The functions, the threshold and the timing of the two interrupt pins (INT1_A/M, INT2_A/M and INT1_G, DRDY_G/INT2_G) can be completely programmed by the user through the I^2C/SPI interfaces.

5.2 Pull-up resistors

If an I^2C interface is used, pull-up resistors (suggested value 10 kOhm) must be placed on the two I^2C bus lines.

5.3 Digital interface power supply

This digital interface dedicated to the linear acceleration and to the magnetic field signal is capable of operating with a standard power supply (Vdd) or using a dedicated power supply (Vdd_IO).

5.4 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

5.5 High current wiring effects

High current in the wiring and printed circuit trace may cause errors in magnetic field measurements for compassing.

Conductor generated magnetic fields add to the earth’s magnetic field making errors in the compass heading computation.

Keep currents higher than 10 mA a few millimeters further away from the sensor IC.

6 Digital interfaces

The registers embedded in the LSM333D may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

To select/exploit the I^2C interface, the CS line must be tied HIGH (i.e. connected to Vdd_IO).

Table 9. Serial interface pin description

Pin name	Pin description
CS_A/M	Linear acceleration SPI enable Linear acceleration I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
CS_G	Angular rate SPI enable Angular rate I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
SCL	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SDO_A/M SDO_G	I^2C least significant bit of the device address (SA0) SPI serial data output (SDO)

6.1 I^2C serial interface

The LSM333D I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 10. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bi-directional line used for sending and receiving the data to/from the interface. Both lines must be connected to Vdd_IO through external pull-up resistors. When the bus is free, both lines are HIGH.

The I^2C interface is compliant with Fast mode (400 kHz) I^2C standards as well as with Normal mode.

6.1.1 I²C Operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the START condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first 7 bits after a START condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LSM333D is 00111xxb, whereas the xx bits are modified by the SDO/SA0 pin in order to modify the device address. If the SEL pin is connected to the voltage supply, the address is 0011101b, otherwise, if the SDO/SA0 pin is connected to ground, the address is 0011110b. This solution allows the connection and addressing of two different accelerometers to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded in the LSM333D behaves as a slave device and the following protocol must be adhered to. After the START condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address is transmitted: the 7 LSb represent the actual register address while the MSb enables address auto-increment. If the MSb of the SUB field is 1, the SUB (register address) is automatically incremented to allow multiple data read/write.

The slave address is completed with a read/write bit. If the bit is ‘1’ (read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is ‘0’ (write) the master transmits to the slave with direction unchanged. *Table 11* and *Table 12* explain how the SAD+read/write bit pattern is composed, listing all the possible configurations.

Table 11. eCompass SAD+read/write patterns

Command	SDO/SA0 pin	SAD[6:2]	SAD[1:0]	R/W	SAD+R/W
Read	0	00111	10	1	3D
Write	0	00111	10	0	3C
Read	1	00111	01	1	3B
Write	1	00111	01	0	3A

Table 12. Angular rate SAD+read/write patterns

Command	SAD[6:1]	SAD[0] = SDO_G pin	R/W	SAD+R/W
Read	110101	0	1	D5
Write	110101	0	0	D4
Read	110101	1	1	D7
Write	110101	1	0	D6

Table 13. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 14. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 15. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 16. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data is transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes sent per transfer is unlimited. Data is transferred with the most significant bit (MSb) first. If a receiver cannot receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL, LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver does not acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to ‘1’ while SUB(6-0) represents the address of the first register to be read.

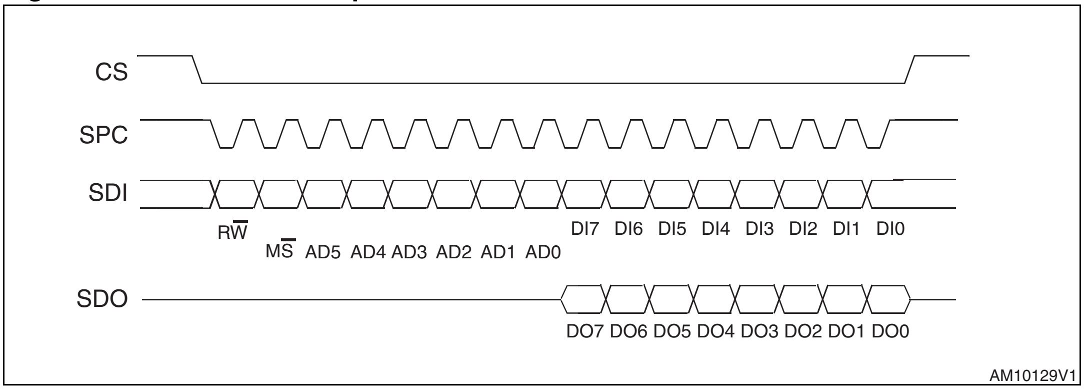
In the communication format presented, MAK is master acknowledge and NMAK is no master acknowledge.

6.2 SPI bus interface

The SPI is a bus slave. The SPI allows the writing and reading of the registers of the device.

The serial interface interacts with the outside world through 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 14. Read and write protocol



CS is the serial port enable and is controlled by the SPI master. It goes LOW at the start of the transmission and returns HIGH at the end. **SPC** is the serial port clock and is controlled by the SPI master. It is stopped HIGH when **CS** is HIGH (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in the case of multiple bytes read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written to the device. When 1, the data DO(7:0) from the device is read. In the latter case, the chip drives **SDO** at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address is auto-incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (Write mode). This is the data that is written to the device (MSb first).

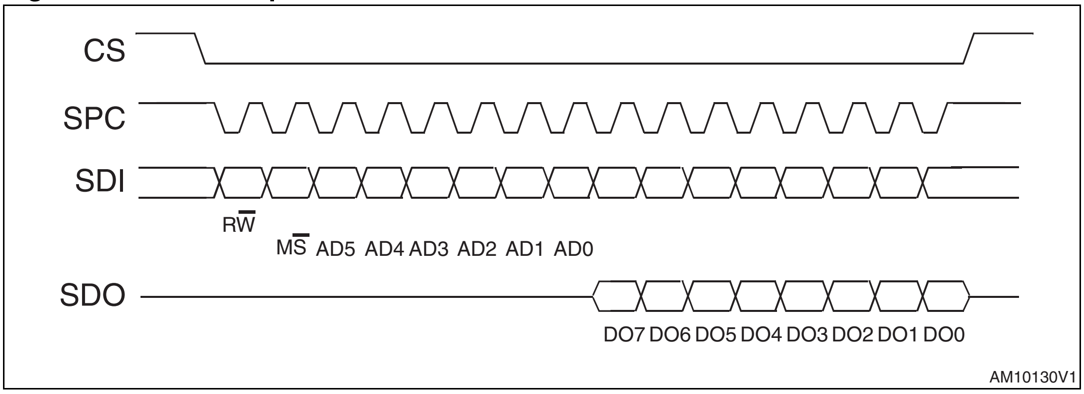
bit 8-15: data DO(7:0) (Read mode). This is the data that is read from the device (MSb first).

In multiple read/write commands, further blocks of 8 clock periods are added. When the M$\overline{S}$ bit is 0, the address used to read/write data remains the same for every block. When the M$\overline{S}$ bit is 1, the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

6.2.1 SPI read

Figure 15. SPI read protocol



The SPI read command is performed with 16 clock pulses. The multiple byte read command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: READ bit. The value is 1.

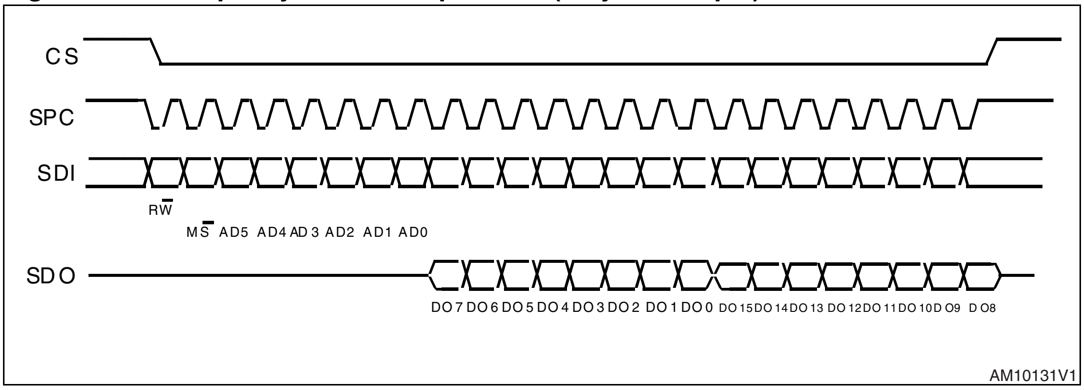
bit 1: $M\overline{S}$ bit. When 0, do not increment address; when 1, increment address in multiple readings.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (Read mode). This is the data that is read from the device (MSb first).

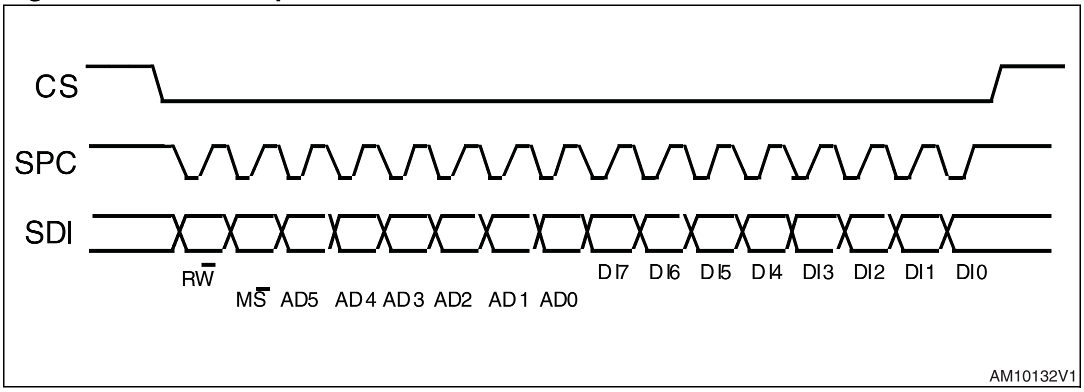
bit 16-... : data DO(...-8). Further data in multiple byte readings.

Figure 16. Multiple byte SPI read protocol (2-byte example)



6.2.2 SPI write

Figure 17. SPI write protocol



The SPI write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

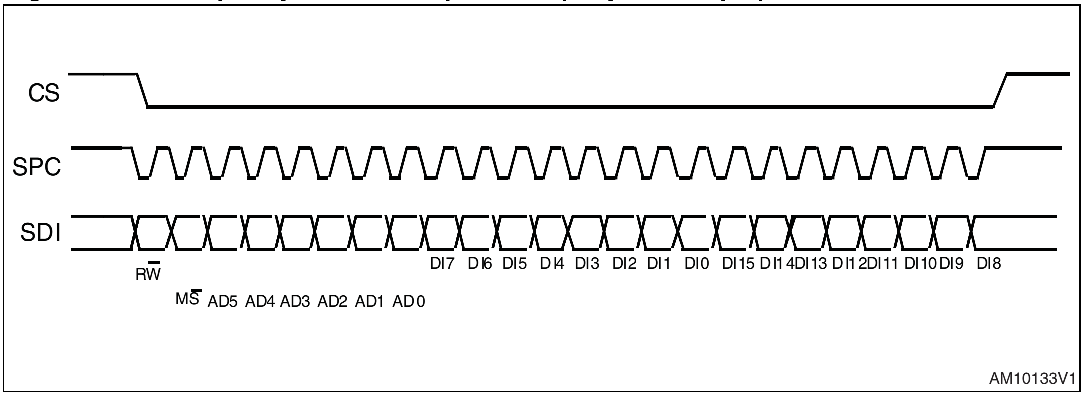
bit 1: M$\overline{S}$ bit. When 0, do not increment address; when 1, increment address in multiple writings.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (Write mode). This is the data that is written to the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writings.

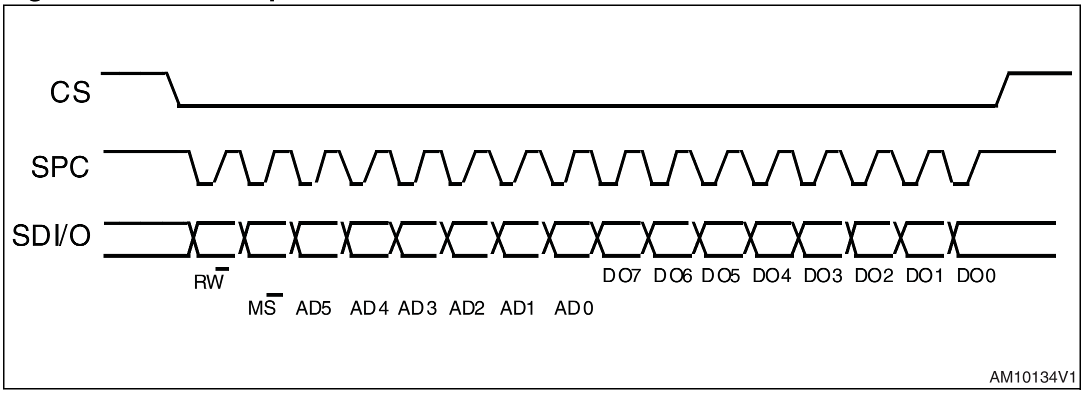
Figure 18. Multiple byte SPI write protocol (2-byte example)



6.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the bit SIM (SPI serial interface mode selection) to '1' in *CNTRL2_A (21 h)*.

Figure 19. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: $M\overline{S}$ bit. When 0, do not increment address; when 1, increment address in multiple readings.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (Read mode). This is the data that is read from the device (MSb first).

Multiple read command is also available in 3-wire mode.

7 Output register mapping

The table below provides a listing of the 8-bit registers embedded in the device, and the related addresses:

Table 17. Accelerometer and Magnetometer sensing register address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
Reserved	--	00-04	--	--	Reserved
Reserved	--	05	000 0101	--	Reserved
Reserved	r--	06	000 0110	--	Reserved
STATUS_REG_M	r	07	000 0111	00000000	
OUT_X_L_M	r	08	000 1000	Output	
OUT_X_H_M	r	09	000 1001	Output	
OUT_Y_L_M	r	0A	000 1010	Output	
OUT_Y_H_M	r	0B	000 1011	Output	
OUT_Z_L_M	r	0C	000 1100	Output	
OUT_Z_H_M	r	0D	000 1101	Output	
Reserved	--	0E	000 1110	--	Reserved
WHO_AM_I	r	0F	000 1111	01001001	
Reserved	--	10-11	--	--	Reserved
INT_CTRL_REG_M	rw	12	001 0010	11101000	
INT_SRC_REG_M	r	13	001 0011	00000000	
INT_THS_L_M	rw	14	001 0100	00000000	
INT_THS_H_M	rw	15	001 0101	00000000	
OFFSET_X_L_M	rw	16	001 0110	00000000	
OFFSET_X_H_M	rw	17	001 0111	00000000	
OFFSET_Y_L_M	rw	18	001 01000	00000000	
OFFSET_Y_H_M	rw	19	001 01001	00000000	
OFFSET_Z_L_M	rw	1A	001 01010	00000000	
OFFSET_Z_H_M	rw	1B	001 01011	00000000	
REFERENCE_X	rw	1C	001 01100	00000000	
REFERENCE_Y	rw	1D	001 01101	00000000	
REFERENCE_Z	rw	1E	001 01110	00000000	
CNTRL0_A	rw	1F	001 1111	00000000	
CNTRL1_A	rw	20	010 0000	00000111	
CNTRL2_A	rw	21	010 0001	00000000	

Table 17. Accelerometer and Magnetometer sensing register address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
CNTRL3_A	rw	22	010 0010	00000000	
CNTRL4_A	rw	23	010 0011	00000000	
CNTRL5_A	rw	24	010 0100	00011000	
CNTRL6_A	rw	25	010 0101	00100000	
CNTRL7_A	rw	26	010 0110	00000001	
STATUS_REG_A	r	27	010 0111	00000000	
OUT_X_L_A	r	28	010 1000	Output	
OUT_X_H_A	r	29	010 1001	Output	
OUT_Y_L_A	r	2A	010 1010	Output	
OUT_Y_H_A	r	2B	010 1011	Output	
OUT_Z_L_A	r	2C	010 1100	Output	
OUT_Z_H_A	r	2D	010 1101	Output	
FIFO_CNTRL_REG_A	rw	2E	010 1110	00000000	
FIFO_SRC_REG_A	r	2F	010 1111	00000000	
INT_GEN_1_REG_A	rw	30	011 0000	00000000	
INT_GEN_1_SRC_A	r	31	011 0001	00000000	
INT_GEN_1_THS_A	rw	32	011 0010	00000000	
INT_GEN_1_DURATION_A	rw	33	011 0011	00000000	
INT_GEN_2_REG_A	rw	34	011 0100	00000000	
INT_GEN_2_SRC_A	r	35	011 0101	00000000	
INT_GEN_2_THS_A	rw	36	011 0110	00000000	
INT_GEN_2_DURATION_A	rw	37	011 0111	00000000	
CLICK_CFG_A	rw	38	011 1000	00000000	
CLICK_SRC_A	r	39	011 1001	00000000	
CLICK_THS_A	rw	3A	011 1010	00000000	
TIME_LIMIT_A	rw	3B	011 1011	00000000	
TIME _LATENCY_A	rw	3C	011 1100	00000000	
TIME_WINDOW_A	rw	3D	011 1101	00000000	
Act_THS_A	rw	3E	011 1110	00000000	
Act_DUR_A	rw	3F	011 1111	00000000	

Table 18. Gyroscope sensing register address map

Name	Type	Register address		Default
		Hex	Binary	
Reserved	-	00-0E	-	-
WHO_AM_I	r	0F	000 1111	11010100
Reserved	-	10-1F	-	-
CNTRL1_G	rw	20	010 0000	00000111
CNTRL2_G	rw	21	010 0001	00000000
CNTRL3_G	rw	22	010 0010	00000000
CNTRL4_G	rw	23	010 0011	00000000
CNTRL5_G	rw	24	010 0100	00000000
REFERENCE_G	rw	25	010 0101	00000000
OUT_TEMP_G	r	26	010 0110	Output
STATUS_REG_G	r	27	010 0111	Output
OUT_X_L_G	r	28	010 1000	Output
OUT_X_H_G	r	29	010 1001	Output
OUT_Y_L_G	r	2A	010 1010	Output
OUT_Y_H_G	r	2B	010 1011	Output
OUT_Z_L_G	r	2C	010 1100	Output
OUT_Z_H_G	r	2D	010 1101	Output
FIFO_CTRL_REG_G	rw	2E	010 1110	00000000
FIFO_SRC_REG_G	r	2F	010 1111	Output
INT1_CFG_G	rw	30	011 0000	00000000
INT1_SRC_G	r	31	011 0001	Output
INT1_TSH_XH_G	rw	32	011 0010	00000000
INT1_TSH_XL_G	rw	33	011 0011	00000000
INT1_TSH_YH_G	rw	34	011 0100	00000000
INT1_TSH_YL_G	rw	35	011 0101	00000000
INT1_TSH_ZH_G	rw	36	011 0110	00000000
INT1_TSH_ZL_G	rw	37	011 0111	00000000
INT1_DURATION_G	rw	38	011 1000	00000000

Registers marked as *Reserved* must not be changed. Writing to these registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

8 Register description

The device contains a set of registers which are used to control its behavior and to retrieve acceleration and magnetic data. The register address, consisting of 7 bits, is used to identify them and to write the data through the serial interface.

8.1 Accelerometer and Magnetometer register description

8.2 STATUS_REG_M (07h)

Table 19. STATUS_REG_M register

ZYXMOR/ Tempor	ZMOR	YMOR	XMOR	ZYXMDA / Tempda	ZMDA	YMDA	XMDA

Table 20. STATUS_REG_M description

ZYXMOR/ Tempor	Magnetic X, Y and Z-axis and temperature data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous ones) Temperature data overrun if the TONLY bit in *CNTRL7_A (26h)* is set to ‘1’. Default value:0.
ZMOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the Z-axis has overwritten the previous one)
YMOR	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the Y-axis has overwritten the previous one)
XMOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the X-axis has overwritten the previous one)
ZYXMDA / Tempda	X, Y and Z-axis and temperature new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available) Temperature new data available if the TONLY bit in *CNTRL7_A (26h)* is set to ‘1’. Default value: 0.
ZMDA	Z-axis new data available. Default value: 0 (0: a new data for the Z-axis is not yet available; 1: a new data for the Z-axis is available)
YMDA	Y-axis new data available. Default value: 0 (0: a new data for the Y-axis is not yet available; 1: a new data for the Y-axis is available)
XMDA	X-axis new data available. Default value: 0 (0: a new data for the X-axis is not yet available; 1: a new data for the X-axis is available)

8.3 OUT_X_L_M (08h), OUT_X_H_M (09h)

X-axis magnetic data.

The value is expressed in 16 bits as 2’s complement left justified.

8.4 OUT_Y_L_M (0Ah), OUT_X_H_M (0Bh)

Y-axis magnetic data.

The value is expressed in 16 bits as 2’s complement left justified.

8.5 OUT_X_L_M (0Ch), OUT_X_H_M (0Dh)

Z-axis magnetic data.

The value is expressed in 16 bits as 2’s complement left justified.

8.6 WHO_AM_I (0Fh)

Table 21. WHO_AM_I register

0	1	0	0	1	0	0	1

Device identification register.

8.7 INT_CTRL_REG_M (12h)

Table 22. INT_CTRL_REG_M register

XMIEN	YMIEN	ZMIEN	PP_OD	MIEA	MIEL	4D	MIEN

Table 23. INT_CTRL_REG_M description

XMIEN	Enable interrupt recognition on X-axis for magnetic data. Default value: 0. (0: disable interrupt recognition;1: enable interrupt recognition)
YMIEN	Enable interrupt recognition on Y-axis for magnetic data. Default value: 0. (0: disable interrupt recognition;1: enable interrupt recognition)
ZMIEN	Enable interrupt recognition on Z-axis for magnetic data. Default value: 0. (0: disable interrupt recognition;1: enable interrupt recognition)
PP_OD	Interrupt pin configuration. Default value: 0. (0: push-pull; 1: open drain)
MIEA	Interrupt polarity. Default value: 0. (0: interrupt active low; 1: interrupt active high)

Table 23. INT_CTRL_REG_M description (continued)

MIEL	Latch interrupt request on the *INT_SRC_REG_M (13h)* register. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched) Once the MIEL is set to ‘1’ the interrupt is cleared by reading the *INT_SRC_REG_M (13h)* register.
4D	4D enable: 4D detection on acceleration data is enabled when 6D bit in *INT_GEN_1_REG_A (2Fh)* is set to 1.
MIEN	Enable interrupt generation for magnetic data. Default value: 0. (0: disable interrupt generation;1: enable interrupt generation)

8.8 INT_SRC_REG_M (13h)

Table 24. INT_SRC_REG_M register

M_PTH_X	M_PTH_Y	M_PTH_Z	M_NTH_X	M_NTH_Y	M_NTH_Z	MROI	MINT

Table 25. INT_SRC_REG_M description

M_PTH_X	Magnetic value on X-axis exceeds the threshold on the positive side. Default value: 0.
M_PTH_Y	Magnetic value on Y-axis exceeds the threshold on the positive side. Default value: 0.
M_PTH_Z	Magnetic value on Z-axis exceeds the threshold on the positive side. Default value: 0.
M_NTH_X	Magnetic value on X-axis exceeds the threshold on the negative side. Default value: 0.
M_NTH_Y	Magnetic value on Y-axis exceeds the threshold on the negative side. Default value: 0.
M_NTH_Z	Magnetic value on Z-axis exceeds the threshold on the negative side. Default value: 0.
MROI	Internal measurement range overflow on magnetic value. Default value: 0.
MINT	Magnetic interrupt event. The magnetic field value exceeds the threshold. Default value: 0.

8.9 INT_THS_L_M (14h), INT_THS_H_M (15h)

Magnetic interrupt threshold. Default value: 0.

The value is expressed in 16 bits unsigned.

Even if the threshold is expressed in an absolute value, the device detects both positive and negative threshold.

8.10 OFFSET_X_L_M (16h), OFFSET_X_H_M (17h)

Magnetic offset for X-axis. Default value: 0.

The value is expressed in 16 bits as 2’s complement left justified.

8.11 OFFSET_Y_L_M (18h), OFFSET_Y_H_M (19h)

Magnetic offset for Z-axis. Default value: 0.

The value is expressed in 16 bits as 2’s complement left justified.

8.12 OFFSET_Z_L_M (1Ah), OFFSET_Z_H_M (1Bh)

Magnetic offset for Y-axis. Default value: 0.

The value is expressed in 16 bits as 2’s complement left justified.

8.13 REFERENCE_X (1Ch)

Reference value for high-pass filter for X-axis acceleration data.

8.14 REFERENCE_Y (1Dh)

Reference value for high-pass filter for Y-axis acceleration data.

8.15 REFERENCE_Z (1Eh)

Reference value for high-pass filter for Z-axis acceleration data.

8.16 CNTRL0_A (1Fh)

Table 26. CNTRL0_A register

BOOT	FIFO_EN	WTM_EN	0(1)	0(1)	HP_Click	HPIS1	HPIS2

1. These bits must be set to ‘0’ for the correct working of the device

Table 27. CNTRL0_A description

BOOT	Reboot memory content. Default value: 0 (0: Normal mode; 1: reboot memory content)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disable; 1: FIFO enable)
WTM_EN	FIFO programmable watermark enable. Default value: 0 (0: disable; 1: enable)
HP_Click	High-pass filter enabled for click function. Default value: 0 (0: filter bypassed; 1: filter enabled)
HPIS1	High-pass filter enabled for interrupt generator 1. Default value: 0 (0: filter bypassed; 1: filter enabled)
HPIS2	High-pass filter enabled for interrupt generator 2. Default value: 0 (0: filter bypassed; 1: filter enabled)

8.17 CNTRL1_A (20h)

Table 28. CNTRL1_A register

AODR3	AODR2	AODR1	AODR0	BDU	AZEN	AYEN	AXEN

Table 29. CNTRL0_A description

AODR3-0	Acceleration data rate selection. Default value: 0000 (0000: Power-down mode; Others: refer to *Table 30: Acceleration data rate configuration*)
BDU	Block data update for acceleration and magnetic data. Default value: 0 (0: continuous update; 1: output registers not updated until MSB and LSB have been read)
AZEN	Acceleration Z-axis enable. Default value: 1 (0: Z-axis disabled; 1: Z-axis enabled)
AYEN	Acceleration Y-axis enable. Default value: 1 (0: Y-axis disabled; 1: Y-axis enabled)
AXEN	Acceleration X-axis enable. Default value: 1 (0: X-axis disabled; 1: X-axis enabled)

ODR_A<3:0> is used to set the Power mode and ODR selection. All frequencies resulting in a combination of ODR<3:0> are shown in *Table 30*:

Table 30. Acceleration data rate configuration

AODR3	AODR2	AODR1	AODR0	Power mode selection
0	0	0	0	Power-down mode
0	0	0	1	3.125 Hz
0	0	1	0	6.25 Hz
0	0	1	1	12.5 Hz
0	1	0	0	25 Hz
0	1	0	1	50 Hz
0	1	1	0	100 Hz
0	1	1	1	200 Hz
1	0	0	0	400 Hz
1	0	0	1	800 Hz
1	0	1	0	1600 Hz

8.18 CNTRL2_A (21h)

Table 31. CNTRL2 register

ABW1	ABW0	ABW0	AFS1	AFS0	0[(1)]	AST	SIM

1. This bit must be set to '0' for the correct working of the device

Table 32. CNTRL2_A description

ABW1-0	Accelerometer anti-alias filter bandwidth. Default value: 0 Refer to *Table 33: Acceleration anti-alias filter bandwidth*
AFS	Acceleration full-scale selection. Default value: 00 Refer to *Table 34: Acceleration full-scale selection*
AST	Acceleration self-test enable. Default value: 0 (0: self-test disabled; 1: self-test enabled)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface).

Table 33. Acceleration anti-alias filter bandwidth

ABW1	ABW0	Anti-alias filter bandwidth
0	0	773 Hz
0	1	362 Hz
1	0	194 Hz
1	1	50 Hz

Table 34. Acceleration full-scale selection

AF1	AF0	Acceleration full-scale
0	0	± 2 g
0	1	± 4 g
1	0	± 8 g
1	1	± 16 g

8.19 CNTRL3_A (22h)

Table 35. CNTRL3_A register

P1_BOOT	P1_TAP	P1_INT1	P1_INT2	P1_INTM	P1_DRDYA	P1_DRDYM	P1_EMPTY

Table 36. CNTRL3_A description

P1_BOOT	Boot on INT1 pin enable. Default value: 0 (0: disable; 1: enable)
P1_TAP	Tap generator interrupt on INT1 pin. Default value: 0 (0: disable; 1: enable)
P1_INT1	Inertial interrupt generator 1 on INT1 pin. Default value: 0 (0: disable; 1: enable)
P1_INT2	Inertial interrupt generator 2 on INT1 pin. Default value: 0 (0: disable; 1: enable)
P1_INTM	Magnetic interrupt generator on INT1 pin. Default value: 0 (0: disable; 1: enable)
P1_DRDYA	Accelerometer data-ready signal on INT1 pin. Default value: 0 (0: disable; 1: enable)
P1_DRDYM	Magnetometer data-ready signal on INT1 pin. Default value: 0 (0: disable; 1: enable)
P1_EMPTY	FIFO empty indication on INT1 pin. Default value: 0 (0: disable; 1: enable)

8.20 CNTRL4_A (23h)

Table 37. CNTRL4_A register

P2_TAP	P2_INT1	P2_INT2	P2_INTM	P2_DRDYA	P2_DRDYM	P2_Overrun	P2_WTM

Table 38. CNTRL4_A description

P2_TAP	Tap generator interrupt on INT2 pin. Default value: 0 (0: disable; 1: enable)
P2_INT1	Inertial interrupt generator 1 on INT2 pin. Default value: 0 (0: disable; 1: enable)
P2_INT2	Inertial interrupt generator 2 on INT2 pin. Default value: 0 (0: disable; 1: enable)
P2_INTM	Magnetic interrupt generator on INT2 pin. Default value: 0 (0: disable; 1: enable)
P2_DRDYA	Accelerometer data-ready signal on INT2 pin. Default value: 0 (0: disable; 1: enable)
P2_DRDYM	Magnetometer data-ready signal on INT2 pin. Default value: 0 (0: disable; 1: enable)

Table 38. CNTRL4_A description (continued)

P2_Overrun	FIFO overrun interrupt on INT2 pin. Default value: 0 (0: disable; 1: enable)
P2_WTM	FIFO watermark interrupt on INT2 pin. Default value: 0 (0: disable; 1: enable)

8.21 CNTRL5_A (24h)

Table 39. CNTRL5_A register

1(1)	1(1)	1(1)	M_ODR2	M_ODR1	M_ODR0	LIR2	LIR1

1. These bits must be set to ‘1’ for the correct working of the device.

Table 40. CNTRL5_A description

M_ODR2-0	Magnetic data rate selection. Default value: 110 Refer to *Table 41: Magnetic data rate configuration*
LIR2	Latch interrupt request on INT2_SRC register, with INT2_SRC register cleared by reading INT2_SRC itself. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched)
LIR1	Latch interrupt request on INT1_SRC register, with INT1_SRC register cleared by reading INT1_SRC itself. Default value: 0. (0: interrupt request not latched; 1: interrupt request latched).

Table 41. Magnetic data rate configuration

MODR2	MODR1	MODR0	Power mode selection
0	0	0	3.125 Hz
0	0	1	6.25 Hz
0	1	0	12.5 Hz
0	1	1	25 Hz
1	0	0	50 Hz
1	0	1	100 Hz
1	1	0	200 Hz
1	1	1	Reserved

8.22 CNTRL6_A (25h)

Table 42. CNTRL6_A register

0(1)	MFS1	MFS0	0(1)	0(1)	0(1)	0(1)	0(1)

1. These bits must be set to ‘0’ for the correct working of the device.

Table 43. **CNTRL6_A_ description**

MFS1-0	Magnetic full-scale selection. Default value: 01 Refer to *Table 44: Magnetic full-scale selection*

Table 44. **Magnetic full-scale selection**

MFS1	MFS0	Magnetic full-scale
0	0	± 2 gauss
0	1	± 4 gauss
1	0	± 8 gauss
1	1	± 12 gauss

8.23 CNTRL7_A (26h)

Table 45. **CNTRL7_A register**

AHPM1	AHPM0	AFDS	0(1)	0(1)	MLP	MD1	MD0

1. This bit must be set to '0' for the correct working of the device.

Table 46. **CNTRL7_A description**

AHPM1-0	High-pass filter mode selection for acceleration data. Default value: 00 Refer to *Table 47: High-pass filter mode selection*
AFDS	Filtered acceleration data selection. Default value: 0 (0: internal filter bypassed; 1: data from internal filter sent to output register and FIFO)
MLP	Magnetic data low power mode. Default value: 0 If this bit is '1', the MODR is set to 3.125 Hz independently from the MODR settings. Once the bit is set to '0', the magnetic data rate is configured by MODR bits in the *CNTRL5_A (24h)* register.
MD1-0	Magnetic sensor mode selection. Default 10 Refer to *Table 48: Magnetic sensor mode selection*

Table 47. **High-pass filter mode selection**

AHPM1	AHPM0	High pass filter mode
0	0	Normal mode (reset X, Y and Z-axis reading *REFERENCE_X (1Ch)*, *REFERENCE_Y (1Dh)* and *REFERENCE_Y (1Dh)* register respectively)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Auto-reset on interrupt event

Table 48. **Magnetic sensor mode selection**

MD1-0	MD1-0	Magnetic sensor mode
0	0	Continuous-conversion mode
0	1	Single-conversion mode
1	0	Power-down mode
1	1	Power-down mode

8.24 STATUS_REG_A (27h)

Table 49. **STATUS_REG_A register**

ZYXAOR	ZAOR	YAOR	XAOR	ZYXADA	ZADA	YADA	XADA

Table 50. **STATUS_REG_A description**

ZYXAOR/	Acceleration X, Y and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous ones)
ZAOR	Acceleration Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the Z-axis has overwritten the previous one)
YAOR	Acceleration Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the Y-axis has overwritten the previous one)
XAOR	Acceleration X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the X-axis has overwritten the previous one)
ZYXADA	Acceleration X, Y and Z-axis new value available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZADA	Acceleration Z-axis new value available. Default value: 0 (0: a new data for the Z-axis is not yet available; 1: a new data for the Z-axis is available)
YADA	Acceleration Y-axis new value available. Default value: 0 (0: a new data for the Y-axis is not yet available; 1: a new data for the Y-axis is available)
XADA	Acceleration X-axis new value available. Default value: 0 (0: a new data for the X-axis is not yet available; 1: a new data for the X-axis is available)

8.25 OUT_X_L_A (28h), OUT_X_H_A (29h)

X-axis acceleration data.

The value is expressed in 16 bits as 2's complement left justified.

8.26 OUT_Y_L_A (2Ah), OUT_X_H_A (2Bh)

Y-axis acceleration data.

The value is expressed in 16 bits as 2's complement left justified.

8.27 OUT_X_L_A (2Ch), OUT_X_H_A (2Dh)

Z-axis acceleration data.

The value is expressed in 16 bits as 2's complement left justified.

8.28 FIFO_CNTRL_REG_A (2Eh)

Table 51. FIFO_CTRL_REG_A register

FM2	FM1	FM0	FTH4	FTH3	FTH2	FTH1	FTH0

Table 52. FIFO_CTRL_REG_A register description

FM1-FM0	FIFO mode selection. Default value: 000 Refer to *Table :*
FTH4:0	FIFO watermark level. Default value: 0000

Table 53. FIFO mode configuration

FM2	FM1	FM0	FIFO mode
0	0	0	Bypass mode
0	0	1	FIFO mode
0	1	0	Stream mode
0	1	1	Stream-to-FIFO mode
1	0	0	Bypass-to-stream mode

Interrupt generator 2 can change the FIFO mode.

8.29 FIFO_SRC_REG_A (2Fh)

Table 54. FIFO_SRC_REG_A register

WTM	OVRN	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 55. **FIFO_SRC_REG_A description**

WTM	Watermark status. WTM bit is set to ‘1’ when FIFO content exceeds watermark level.
OVRN	FIFO overrun status. OVRN bit is set to ‘1’ when FIFO buffer is full.
EMPTY	Empty status. EMPTY bit is set to ‘1’ when all FIFO samples have been read and FIFO is empty.
FSS4-0	FIFO stored data level. FSS4-0 bits contain the current number of unread FIFO levels.

8.30 INT_GEN_1_REG_A (2Fh)

This register contains the settings for the inertial interrupt generator 1.

Table 56. **INT_GEN_1_REG_A register**

AOI	6D	ZHIE/ ZUPE	ZLIE/ ZDOWNE	YHIE/ YUPE	YLIE/ YDOWNE	XHIE/ XUPE	XLIE/ XDOWNE

Table 57. **INT_GEN_1_REG_A description**

AOI	AND/OR combination of interrupt events. Default value: 0. Refer to *Table 58, "Interrupt mode"*
6D	6-direction detection function enabled. Default value: 0. Refer to *Table 58, "Interrupt mode"*
ZHIE/ ZUPE	Enable interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request;1: enable interrupt request)
ZLIE/ ZDOWNE	Enable interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request;1: enable interrupt request)
YHIE/ YUPE	Enable interrupt generation on Y high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
YLIE/ YDOWNE	Enable interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XHIE/ XUPE	Enable interrupt generation on X high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XLIE/XDOWN E	Enable interrupt generation on X low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)

Content of this register is loaded at boot.

Write operation at this address is possible only after system boot.

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Table 58. Interrupt mode

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6-direction movement recognition
1	0	AND combination of interrupt events
1	1	6-direction position recognition

Difference between AOI-6D = ‘01’ and AOI-6D = ‘11’.

AOI-6D = ‘01’ is movement recognition. An interrupt is generated when orientation moves from an unknown zone to a known zone. The interrupt signal stays for a duration ODR.

AOI-6D = ‘11’ is direction recognition. An interrupt is generated when orientation is inside a known zone. The interrupt signal stays until orientation is inside the zone.

8.31 INT_GEN_1_SRC_A (31h)

This register contains the status for the inertial interrupt generator 1.

Table 59. INT_GEN_1_SRC_A register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 60. INT_GEN_1_SRC_A description

IA	Interrupt status. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Reading at this address clears the *INT_GEN_1_SRC_A (31h)* IA bit (and the interrupt signal on the corresponding interrupt pin) and allows the refreshment of data in the *INT_GEN_1_SRC_A (31h)* register if the latched option was chosen.

8.32 INT_GEN_1_THS_A (32h)

Table 61. INT1_THS register_A

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 62. INT1_THS description_A

THS6 - THS0	Interrupt 1 threshold. Default value: 000 0000

8.33 INT_GEN_1_DURATION_A (33h)

Table 63. INT1_DURATION_A register

0	D6	D5	D4	D3	D2	D1	D0

Table 64. INT1_DURATION_A description

D6 - D0	Duration value. Default value: 000 0000

D6 - D0 bits set the minimum duration of the interrupt 1 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

8.34 INT_GEN_2_REG_A (34h)

This register contains the settings for the inertial interrupt generator 2.

Table 65. INT_GEN_2_REG_A register

AOI	6D	ZHIE/ ZUPE	ZLIE/ ZDOWNE	YHIE/ YUPE	YLIE/ YDOWNE	XHIE/ XUPE	XLIE/ XDOWNE

Table 66. INT_GEN_2_REG_A description

AOI	AND/OR combination of interrupt events. Default value: 0. Refer to *Table 66, "INT_GEN_2_REG_A description"*
6D	6-direction detection function enabled. Default value: 0. Refer to *Table 66, "INT_GEN_2_REG_A description"*
ZHIE/ ZUPE	Enable interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request;1: enable interrupt request)
ZLIE/ ZDOWNE	Enable interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request;1: enable interrupt request)
YHIE/ YUPE	Enable interrupt generation on Y high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
YLIE/ YDOWNE	Enable interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)

Table 66. INT_GEN_2_REG_A description (continued)

XHIE/ XUPE	Enable interrupt generation on X high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)
XLIE/XDOWN E	Enable interrupt generation on X low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request.)

Content of this register is loaded at boot.

Write operation at this address is possible only after system boot.

Table 67. Interrupt mode

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6-direction movement recognition
1	0	AND combination of interrupt events
1	1	6-direction position recognition

Difference between AOI-6D = ‘01’ and AOI-6D = ‘11’.

AOI-6D = ‘01’ is movement recognition. An interrupt is generated when orientation moves from an unknown zone to a known zone. The interrupt signal stays for a duration ODR.

AOI-6D = ‘11’ is direction recognition. An interrupt is generated when orientation is inside a known zone. The interrupt signal stays until orientation is inside the zone.

8.35 INT_GEN_2_SRC_A (35h)

This register contains the status for the inertial interrupt generator 2.

Table 68. INT_GEN_2_SRC_A register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 69. INT_GEN_2_SRC_A description

IA	Interrupt status. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt, 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)

Table 69. INT_GEN_2_SRC_A description (continued)

YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: x high event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Reading at this address clears the *INT_GEN_2_SRC_A (35h)* IA bit (and the interrupt signal on the corresponding interrupt pin) and allows the refreshment of data in the *INT_GEN_2_SRC_A (35h)* register if the latched option was chosen.

8.36 INT_GEN_2_THS_A (36h)

Table 70. INT_GEN_2_THS_A register

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 71. INT_GEN_2_THS_A description

THS6 - THS0	Interrupt 1 threshold. Default value: 000 0000

8.37 INT_GEN_2_DURATION_A (37h)

Table 72. INT_GEN_2_DURATION_A register

0	D6	D5	D4	D3	D2	D1	D0

Table 73. INT_GEN_2_DURATION_A description

D6 - D0	Duration value. Default value: 000 0000

D6 - D0 bits set the minimum duration of the interrupt 2 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

8.38 CLICK_CFG_A (38h)

Table 74. CLICK_CFG_A register

--	--	ZD	ZS	YD	YS	XD	XS

Table 75. CLICK_CFG_A description

ZD	Enable interrupt double tap-tap on Z-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
ZS	Enable interrupt single tap-tap on Z-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YD	Enable interrupt double tap-tap on Y-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YS	Enable interrupt single tap-tap on Y-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XD	Enable interrupt double tap-tap on X-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XS	Enable interrupt single tap-tap on X-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)

8.39 CLICK_SRC_A (39h)

Table 76. CLICK_SRC_A register

--	IA	DClick	SClick	Sign	Z	Y	X

Table 77. CLICK_SRC_A description

--	-
IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
DClick	Double click-click enable. Default value: 0 (0: double click-click detection disable, 1: double tap-tap detection enable)
Stap	Single click-click enable. Default value: 0 (0: single click-click detection disable, 1: single click-click detection enable)
Sign	Click-click sign. 0: positive detection, 1: negative detection
Z	Z click-click detection. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
Y	Y click-click detection. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
X	X click-click detection. Default value: 0 (0: no interrupt, 1: X high event has occurred)

8.40 CLICK_THS_A (3Ah)

Table 78. CLICK_THS_A register

-	Ths6	Ths5	Ths4	Ths3	Ths2	Ths1	Ths0

Table 79. CLICK_SRC_A description

Ths6-Ths0	Click-click threshold. Default value: 000 0000

8.41 TIME_LIMIT_A (3Bh)

Table 80. TIME_LIMIT_A register

-	TLI6	TLI5	TLI4	TLI3	TLI2	TLI1	TLI0

Table 81. TIME_LIMIT_A description

TLI7-TLI0	Click-click time limit. Default value: 000 0000

8.42 TIME_LATENCY_A (3Ch)

Table 82. TIME_LATENCY_A register

TLA7	TLA6	TLA5	TLA4	TLA3	TLA2	TLA1	TLA0

Table 83. TIME_LATENCY_A description

TLA7-TLA0	Click-click time latency. Default value: 000 0000

8.43 TIME_WINDOW_A (3Dh)

Table 84. TIME_WINDOW_ register

TW7	TW6	TW5	TW4	TW3	TW2	TW1	TW0

Table 85. TIME_WINDOW_A description

TW7-TW0	Click-click time window

8.44 Act_THS_A (3Eh)

Table 86. Act_THS_A register

--	Acth6	Acth5	Acth4	Acth3	Acth2	Acth1	Acth0

Table 87. Act_THS_A description

Acth[6-0]	Sleep-to-Wake, Return to Sleep activation threshold 1LSb = 16mg

8.45 Act_DUR_A (3Fh)

Table 88. Act_DUR_A register

ActD7	ActD6	ActD5	ActD4	ActD3	ActD2	ActD1	ActD0

Table 89. Act_DUR_A description

ActD[7-0]	Sleep-to-Wake, Return to Sleep duration DUR = (Act_DUR + 1)*8/ODR

9 Gyroscope register description

The device contains a set of registers which are used to control its behavior and to retrieve angular rate data. The register address, consisting of 7 bits, is used to identify them and to write the data through the serial interface.

9.1 WHO_AM_I_G (0Fh)

Table 90. WHO_AM_I register

1	1	0	1	0	1	0	0

Device identification register.

9.2 CNTRL1_G (20h)

Table 91. CNTRL1_G register

DR1	DR0	BW1	BW0	PD	Zen	Xen	Yen

Table 92. CNTRL1_G description

DR1-DR0	Output data rate selection. Refer to *Table 93: DR and BW configuration setting*
BW1-BW0	Bandwidth selection. Refer to *Table 93: DR and BW configuration setting*
PD	Power-down mode enable. Default value: 0 (0: Power-down mode, 1: Normal mode or Sleep mode)
Zen	Z-axis enable. Default value: 1 (0: Z-axis disabled; 1: Z-axis enabled)
Yen	Y-axis enable. Default value: 1 (0: Y-axis disabled; 1: Y-axis enabled)
Xen	X-axis enable. Default value: 1 (0: X-axis disabled; 1: X-axis enabled)

DR<1:0> is used for ODR selection. **BW <1:0>** is used for bandwidth selection.

In *Table 93: DR and BW configuration setting*, all frequencies resulting in combinations of DR / BW bits are reported.

Table 93. DR and BW configuration setting

DR <1:0>	BW <1:0>	ODR [Hz]	Cut-Off
00	00	95	12.5
00	01	95	25
00	10	95	25
00	11	95	25
01	00	190	12.5
01	01	190	25
01	10	190	50
01	11	190	70
10	00	380	20
10	01	380	25
10	10	380	50
10	11	380	100
11	00	760	30
11	01	760	35
11	10	760	50
11	11	760	100

A combination of **PD, Zen, Yen, Xen** is used to set the device to different modes (Power-down / Normal / Sleep) in accordance with *Table 94: Power mode selection configuration* below.

Table 94. Power mode selection configuration

Mode	PD	Zen	Yen	Xen
Power-down	0	-	-	-
Sleep	1	0	0	0
Normal	1	-	-	-

9.3 CNTRL2_G (21h)

Table 95. CNTRL2_G register

0(1)	0(1)	HPM1	HPM1	HPCF3	HPCF2	HPCF1	HPCF0

1. These bits must be set to ‘0’ to ensure proper operation of the device.

Table 96. **CNTRL2_G description**

HPM1- HPM0	High-pass filter mode selection. Default value: 00 Refer to *Table 97: High-pass filter mode configuration*
HPCF3- HPCF0	High-pass filter cutoff frequency selection Refer to *Table 98: High-pass filter cutoff frequency configuration [Hz]*

Table 97. **High-pass filter mode configuration**

HPM1	HPM0	High-pass filter mode
0	0	Normal mode (reset reading HP_RESET_FILTER)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Autoreset on interrupt event

Table 98. **High-pass filter cutoff frequency configuration [Hz]**

HPCF3-0	ODR=95 Hz	ODR=190 Hz	ODR=380 Hz	ODR=760 Hz
0000	7.2	13.5	27	51.4
0001	3.5	7.2	13.5	27
0010	1.8	3.5	7.2	13.5
0011	0.9	1.8	3.5	7.2
0100	0.45	0.9	1.8	3.5
0101	0.18	0.45	0.9	1.8
0110	0.09	0.18	0.45	0.9
0111	0.045	0.09	0.18	0.45
1000	0.018	0.045	0.09	0.18
1001	0.009	0.018	0.045	0.09

9.4 CNTRL3_G (22h)

Table 99. **CNTRL3_G register**

I1_Int1	I1_Boot	H_Lactive	PP_OD	I2_DRDY	I2_WTM	I2_ORun	I2_Empty

Table 100. **CNTRL3_G description**

I1_Int1	Interrupt enable on INT1 pin. Default value 0. (0: disable; 1: enable)
I1_Boot	Boot status available on INT1. Default value 0. (0: disable; 1: enable)
H_Lactive	Interrupt active configuration on INT1. Default value 0. (0: high; 1:low)

Table 100. CNTRL3_G description (continued)

PP_OD	Push-pull / open drain. Default value: 0. (0: push- pull; 1: open drain)
I2_DRDY	Date-ready on DRDY/INT2. Default value 0. (0: disable; 1: enable)
I2_WTM	FIFO watermark interrupt on DRDY/INT2. Default value: 0. (0: disable; 1: enable)
I2_ORun	FIFO overrun interrupt on DRDY/INT2. Default value: 0. (0: disable; 1: enable)
I2_Empty	FIFO empty interrupt on DRDY/INT2. Default value: 0. (0: disable; 1: enable)

9.5 CNTRL4_G (23h)

Table 101. CNTRL4_G register

BDU	BLE	FS1	FS0	-	0(1)	0(1)	SIM

1. This value must not be changed.

Table 102. CNTRL4_G description

BDU	Block data update. Default value: 0 (0: continuous update; 1: output registers not updated until MSb and LSb reading)
BLE	Big/little endian data selection. Default value 0. (0: data LSb @ lower address; 1: data MSb @ lower address)
FS1-FS0	Full-scale selection. Default value: 00 (00: 250 dps; 01: 500 dps; 10: 2000 dps; 11: 2000 dps)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface).

9.6 CNTRL5_G (24h)

Table 103. CNTRL5_G register

BOOT	FIFO_EN	--	HPen	INT1_Sel1	INT1_Sel0	Out_Sel1	Out_Sel0

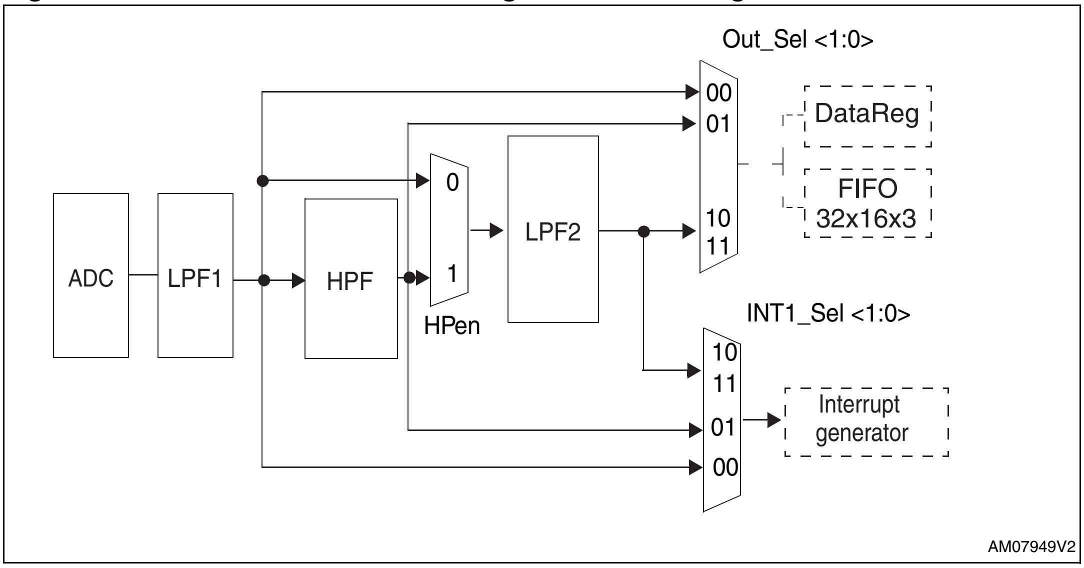
Table 104. CNTRL5_G description

BOOT	Reboot memory content. Default value: 0 (0: Normal mode; 1: reboot memory content)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disable; 1: FIFO enable)
HPen	High-pass filter enable. Default value: 0 (0: HPF disabled; 1: HPF enabled, see *Figure 20*)

Table 104. CNTRL5_G description (continued)

INT1_Sel1- INT1_Sel0	INT1 selection configuration. Default value: 0 (See *Figure 20*)
Out_Sel1- Out_Sel1	Out selection configuration. Default value: 0 (See *Figure 20*)

Figure 20. INT1_Sel and Out_Sel configuration block diagram



9.7 REFERENCE_G (25h)

Table 105. REFERENCE_G register

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0

Table 106. REFERENCE_G register description

Ref 7-Ref0	Reference value for interrupt generation. Default value: 0

9.8 OUT_TEMP_G (26h)

Table 107. OUT_TEMP_G register

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

Table 108. OUT_TEMP_G register description

Temp7-Temp0	Temperature data

Temperature data (1LSB/deg - 8-bit resolution). The value is expressed as 2's complement.

9.9 STATUS_REG_G (27h)

Table 109. STATUS_REG_G register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 110. STATUS_REG_G description

ZYXOR	X, Y, Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data has overwritten the previous data before it was read)
ZOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YOR	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXDA	X, Y, Z-axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z-axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y-axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available;1: new data for the Y-axis is available)
XDA	X-axis new data available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

9.10 OUT_X_L_G (28h), OUT_X_H_G (29h)

X-axis angular rate data. The value is expressed as 2’s complement.

9.11 OUT_Y_L_G (2Ah), OUT_Y_H_G (2Bh)

Y-axis angular rate data. The value is expressed as 2’s complement.

9.12 OUT_Z_L_G (2Ch), OUT_Z_H_G (2Dh)

Z-axis angular rate data. The value is expressed as 2’s complement.

9.13 FIFO_CTRL_REG_G (2Eh)

Table 111. FIFO_CTRL_REG_G register

FM2	FM1	FM0	WTM4	WTM3	WTM2	WTM1	WTM0

Table 112. FIFO_CTRL_REG_G register description

FM2-FM0	FIFO mode selection. Default value: 00 (see *Table 113: FIFO mode configuration*)
WTM4-WTM0	FIFO threshold. Watermark level setting

Table 113. FIFO mode configuration

FM2	FM1	FM0	FIFO mode
0	0	0	Bypass mode
0	0	1	FIFO mode
0	1	0	Stream mode
0	1	1	Stream-to-FIFO mode
1	0	0	Bypass-to-Stream mode

9.14 FIFO_SRC_REG_G (2Fh)

Table 114. FIFO_SRC_REG_G register

WTM	OVRN	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 115. FIFO_SRC_REG_G register description

WTM	Watermark status. (0: FIFO filling is lower than WTM level; 1: FIFO filling is equal or higher than WTM level)
OVRN	Overrun bit status. (0: FIFO is not completely filled; 1:FIFO is completely filled)
EMPTY	FIFO empty bit. (0: FIFO not empty; 1: FIFO empty)
FSS4-FSS1	FIFO stored data level

9.15 INT1_CFG_G (30h)

Table 116. INT1_CFG_G register

AND/OR	LIR	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 117. INT1_CFG_G description

AND/OR	AND/OR combination of interrupt events. Default value: 0 (0: OR combination of interrupt events 1: AND combination of interrupt events
LIR	Latch interrupt request. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched) Cleared by reading INT1_SRC reg.
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)

9.16 INT1_SRC_G (31h)

Interrupt source register. Read only register.

Table 118. INT1_SRC_G register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 119. INT1_SRC_G description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Reading at this address clears the *INT1_SRC_G (31h)* IA bit (and eventually the interrupt signal on the INT1 pin) and allows the refresh of data in the *INT1_SRC_G (31h)* register if the latched option was chosen.

9.17 INT1_THS_XH_G (32h)

Table 120. INT1_THS_XH_G register

-	THSX14	THSX13	THSX12	THSX11	THSX10	THSX9	THSX8

Table 121. INT1_THS_XH_G description

THSX14 - THSX9	Interrupt threshold. Default value: 0000 0000

9.18 INT1_THS_XL_G (33h)

Table 122. INT1_THS_XL_G register

THSX7	THSX6	THSX5	THSX4	THSX3	THSX2	THSX1	THSX0

Table 123. INT1_THS_XL_G description

THSX7 - THSX0	Interrupt threshold. Default value: 0000 0000

9.19 INT1_THS_YH_G (34h)

Table 124. INT1_THS_YH_G register

-	THSY14	THSY13	THSY12	THSY11	THSY10	THSY9	THSY8

Table 125. INT1_THS_YH_G description

THSY14 - THSY9	Interrupt threshold. Default value: 0000 0000

9.20 INT1_THS_YL_G (35h)

Table 126. INT1_THS_YL_G register

THSR7	THSY6	THSY5	THSY4	THSY3	THSY2	THSY1	THSY0

Table 127. INT1_THS_YL_G description

THSY7 - THSY0	Interrupt threshold. Default value: 0000 0000

9.21 INT1_THS_ZH_G (36h)

Table 128. INT1_THS_ZH_G register

-	THSZ14	THSZ13	THSZ12	THSZ11	THSZ10	THSZ9	THSZ8

Table 129. INT1_THS_ZH_G description

THSZ14 - THSZ9	Interrupt threshold. Default value: 0000 0000

9.22 INT1_THS_ZL _G(37h)

Table 130. INT1_THS_ZL_G register

THSZ7	THSZ6	THSZ5	THSZ4	THSZ3	THSZ2	THSZ1	THSZ0

Table 131. INT1_THS_ZL_G description

THSZ7 - THSZ0	Interrupt threshold. Default value: 0000 0000

9.23 INT1_DURATION_G (38h)

Table 132. INT1_DURATION_G register

WAIT	D6	D5	D4	D3	D2	D1	D0

Table 133. INT1_DURATION_G description

WAIT	WAIT enable. Default value: 0 (0: disable; 1: enable)
D6 - D0	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the interrupt event to be recognized. Duration steps and maximum values depend on the ODR chosen.

The **WAIT** bit has the following definitions:

Wait = ‘0’: the interrupt falls immediately if the signal crosses the selected threshold.

Wait = ‘1’: if the signal crosses the selected threshold, the interrupt falls only after the duration has counted the number of samples at the selected data rate, written into the duration counter register.

Figure 21. Wait disabled

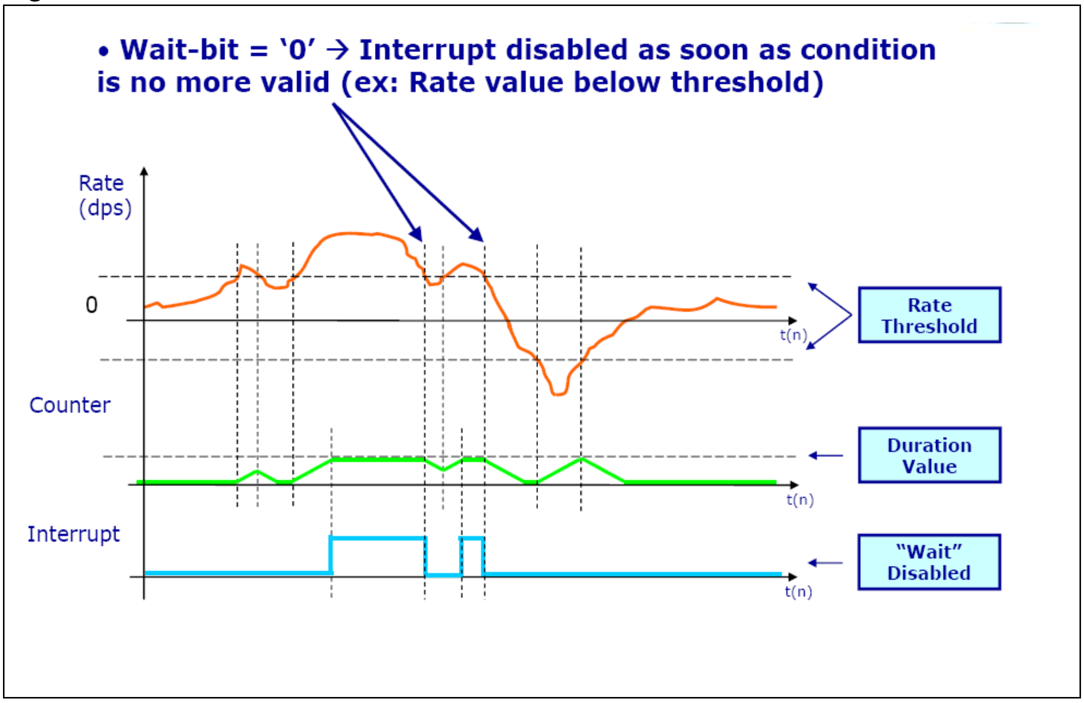
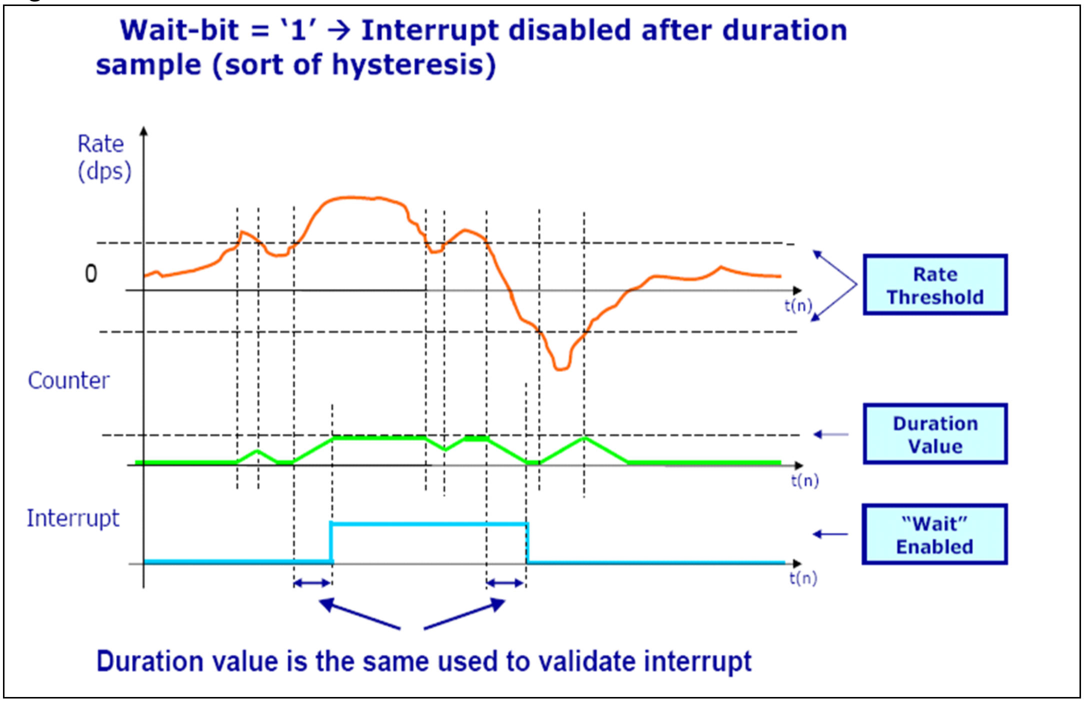


Figure 22. Wait enabled



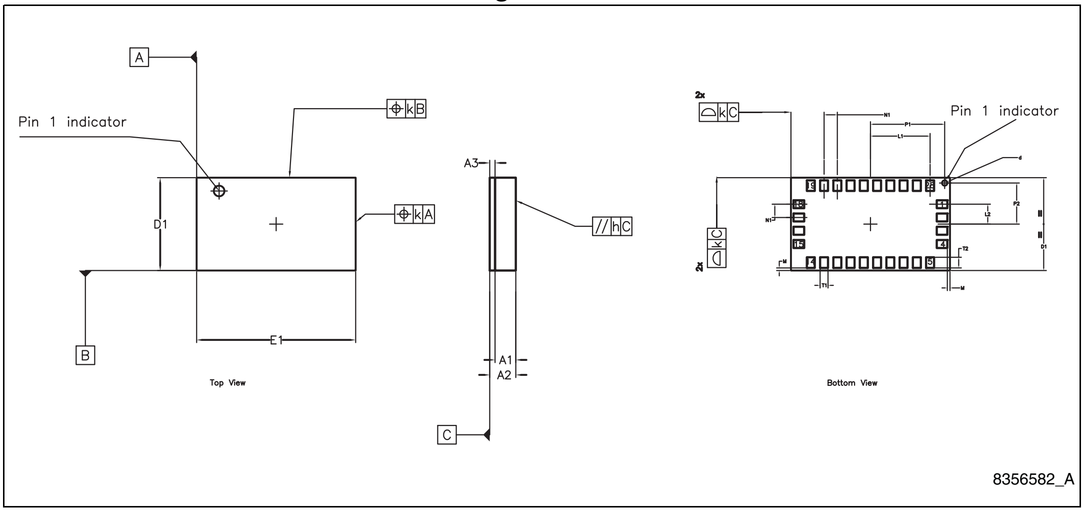
10 Package Information

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Table 134. TFLGA 6x3.5x1 28L mechanical data

Dim.	(mm)		
	Min.	Typ.	Max.
A1		1.000	1.027
A2		0.800	
A3		0.200	
D1	3.350	3.500	3.650
E1	5.850	6.000	6.150
L1		2.250	
L2		0.750	
N1		0.500	
M		0.100	
P1		2.800	
P2		1.550	
T1		0.300	
T2		0.400	
d		0.200	
k		0.050	
h		0.100	

Table 135. TFLGA 6x3.5x1 28L drawing



11 Revision history

Table 136. Document revision history

Date	Revision	Changes
13-Mar-2012	1	Initial release.

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